Synopsys the design partner of choice

2000 Annual Corporate Summary

Synopsys provides the essent
designing and creating the

ial technology and services for
world's most complex chips.

partnering
to inspire
customer
trust

When the question is "How?," the answer is Synopsys

With innovation in the electronics world continuing at a record pace, products like wireless Internet devices, handheld computers and smart appliances are becoming the norm. For the engineering teams who design the chips inside these increasingly essential devices, "How?" has become the multimillion-dollar question. How do they design something that fits millions of tiny transistors and miles of tiny wires on a chip the size of a postage stamp—with no mistakes? How do they verify that such a complex chip will work as specified once it is manufactured and sold? And how do they meet the unforgiving time-to-market goals of competitive global markets?

In every case, the answer is Synopsys. The question of "How?" is answered with software and services that help our customers solve the most difficult design challenges they face each day. At the front end of the design process our flagship product, Design Compiler,™ helps them turn their ideas into logic—the instructions that the chip carries out. At the back end of the design process, our products help determine where millions of transistors will be physically located on the chip. And throughout the design process, our products help customers test, analyze and verify that their chip will work as intended, first time, every time.

That's why virtually every complex chip produced today is designed with at least one Synopsys product. Synopsys has become the trusted design partner to semiconductor and electronics companies alike based on our technology leadership, commitment to excellence and peerless track record of delivering best-in-class results—year after year, chip after chip.

partnering to unleash the potential of customer innovation

The right solution for an increasingly complex job

Physical synthesis

Chip design is at a crossroads. Chip designers are increasingly finding that many of the tools and methods that served them effectively in the past are altogether inadequate to meet the demands of their newest and most complex designs. The reason is that as the size of transistors and wires on a chip shrink, new problems develop. And as the leading edge of chip design moves to silicon technology of 0.18-micron and below, these problems get worse.

Synopsys' solution is to help our customers easily migrate to next-generation design with physical synthesis, a suite of products that solve the problems they are encountering as they create their newest designs. Built to permit a smooth transition from Design Compiler, Physical Compiler™ is the cornerstone of our physical synthesis initiative and has become the fastest growing product in the Company's history.

Physical synthesis is the first and the best technology to address the design needs of the massive 0.18-micron retooling wave that is now underway throughout the IC design community, and Synopsys customers like Cray and NVIDIA are already achieving significant results with it. Physical synthesis is also helping to cut weeks off of many chip design schedules, a benefit that can make the difference between our customers having a competitive product or missing a fast-moving market window altogether.

partners in solving our customers' toughest challenges

Powerful remedies for a persistent bottleneck

Verification

In today's markets, designers don't get a second chance to get a chip right. The costs of a defective chip—whether measured by delay to market, the expense of a product recall or the loss of goodwill—are enormous. That's why our customers go to great lengths to verify that their chips work correctly.

In fact, designers are now taking far longer to confirm that a design functions as specified than they typically take to create the design in the first place. One analyst estimates that up to 70 percent of total design time is now consumed by efforts to verify the most advanced system-on-a-chip designs. Why? Because the verification task multiplies geometrically as the number of transistors on a chip grows. Consequently, the time it takes to verify the functionality of a chip can seriously delay the completion of the overall design if not approached correctly.

Synopsys is easing the verification bottleneck by offering a comprehensive suite of products that help designers work more efficiently by virtue of the speed and accuracy of our market-leading simulators, VCS™ and Scirocco™, and also work smarter through tools like VERA®, Formality® and PrimeTime® that help designers attack their verification challenges in intelligent ways. Our industrial-strength verification solutions are enabling customers to save valuable time and get their products to market more quickly with the confidence that Synopsys understands that ultimate success is always in the details.

accelerating customer results and time to market

Solving the toughest design challenges, one chip at a time

IP and professional services

Among our customers, there's no shortage of innovative ideas to turn silicon into sophisticated products that can increase personal and business productivity, enhance the ways we communicate, entertain us and otherwise enrich our lives. But for the company trying to be first to market with a hot new product, there are never enough engineers to meet an aggressive design schedule.

Synopsys offers products that help our customers use their precious design resources efficiently. We have a large and growing portfolio of high-quality design "building blocks," for example, that customers can use in significant portions of their designs. Every building block that a customer accesses from Synopsys is one less block they have to design from scratch. This enables them to focus more attention and talent on the differentiated chip functions that will make their end products successful.

In addition, Synopsys' professional services organization offers expert assistance to help customers more effectively accomplish their design objectives. By focusing on the hottest market segments, like wireless and broadband, our professional services organization is able to advise, work alongside and/or provide complete turnkey design services for customers seeking to move their products to market faster. We have a team of highly experienced designers working in field offices and design centers strategically located close to our leading customers around the world. Whether through services or advanced technology, Synopsys is committed to solving the toughest design challenges, one chip at a time, wherever our customers require expert attention.

enhancing
our growth
and
strengthening
financial
predictability

New groundwork for solid, predictable growth

Technology subscription licenses

With a strong foundation of well-established, best-in-class products in place and a promising portfolio of new products and services ramping up, Synopsys is well positioned to take advantage of the next wave of silicon-based innovation. In fiscal 2000, we made important changes in the way we license our products that help lay the groundwork for solid, predictable growth in the years ahead.

Historically, software companies have sold their products as "perpetual" licenses under which a customer pays a one-time fee and is entitled to use the product forever. In Q4, we introduced Technology Subscription Licenses (TSLs), under which a customer buys the right to use our software for a fixed period of time, after which they have the opportunity to extend their subscription rights to use the software. TSLs will enable Synopsys to offer our customers technology and terms that more closely match their needs. TSLs will also lead to an improved pricing environment, help us roll out new technology in a more planned manner and give us much greater visibility into our earnings stream.

Finally, because the TSL model realizes revenue over the term of the license rather than upon initial sale, we will enter future quarters with most of our revenue already "locked in" because it will come out of our deferred revenue. With the current retooling wave underway in the semiconductor industry, this puts Synopsys in a strengthened position to capture the full value of our products and services now and in the quarters ahead.

advancing technology means customer success

Cementing our role as “Design Partner of Choice”

Synopsys enters fiscal 2001 with the best technology in the EDA industry, a strong new product pipeline, an expert services organization, a solid, conservative financial footing and a retooling wave that is only now beginning to form.

Similar to the last retooling wave of the late ’80s and early ’90s when semiconductor companies met the challenges of transitioning from 1.0-micron to 0.6-micron design to develop the application specific integrated circuit (ASIC) to its full potential, our customers are now adopting the Synopsys technologies that will help them prosper with current and emerging generations of silicon. Whether measured by customer adoption, orders or chips completed, Synopsys is leading the current wave that will usher in a dazzling new array of advanced electronic products in the months and years ahead.

Our commitment to innovation, excellence and technology leadership are the cornerstones of the partnerships we have established with the world’s leading semiconductor and electronics companies. We will continue to earn their trust by anticipating and helping to solve their most pressing electronic design challenges. As our customers forge ahead into 0.18-micron silicon and beyond, Synopsys intends to continue providing the mission-critical tools and services that cement our role as our customers’ Design Partner of Choice.

Letter to our Shareholders

In every respect, fiscal 2000 was a year of great change and accomplishment for Synopsys. Three years ago we started the transition to become a $1 billion company. Our objectives were straightforward: significantly broaden our market position, increase our customer proximity, transition our software business model to the next generation and upgrade our internal organizational structure and systems. In fiscal 2000, all the pieces came together.

Fiscal 2000, however, was not an easy year. Uncertainty around growth early in the year contributed to a stock decline. Focusing the whole company on the roll-out of physical synthesis, our next-generation product line, forced us to make trade-offs that we had never had to make before. Surrounded by a wave of "dot-com" opportunities, we experienced a spike in turnover. Finally, we managed the Company through a license-model transition.

Looking back, every Synopsys employee is proud that we managed each of these challenges well and that the Company is significantly stronger for it. Our entire focus is now dedicated to growing and broadening Synopsys from a strong product position.

As we pass beyond $1 billion in orders in fiscal 2001, it's worth looking at what it takes to be strong and successful at this level.

Since its inception, Synopsys has endeavored to be a company that is both a major force in the electronics industry and a great place to work. The elements necessary to achieve these objectives are now in place. Let's review each of them:

- Products that meet the market's needs
- A vision for the future of electronic design
- A predictable business model
- A balanced management and employee team
- A field organization with experience, knowledge and a global reach
- Customer relationships based on trust
- An environment of innovation
- A heart and soul for community and employee concerns

Market needs

Let's first take a look at the market. Today, virtually every sophisticated chip in the world is designed using Synopsys software. Our customers differentiate themselves by the speed, power utilization and cost of their chips, as well as by the time it takes them to get to market. These metrics are greatly impacted by the power of the design tools that they use, so it's no surprise that our customers are constantly seeking better tools.

Historically, major retooling among our customers has occurred in waves roughly ten years apart. The last major wave was in the late '80s and early '90s, when customers transitioned from designing chips with 1.0-micron-sized transistors to designing them at 0.6-micron. The old tools weren't sufficient for the new silicon technologies. We at Synopsys were quite familiar with that transition, because our first product, Design Compiler, revolutionized design at that time and brought us to the forefront of electronic design automation (EDA).

The opportunity is very similar now. The transition from designing chips at 0.25-micron to designing them at 0.18-micron is well underway. About 25 percent of new designs are being done at 0.18-micron already. This transition, like the one in the '80s and '90s, has created the need for our customers to retool and to install new software that enables them to design at these new geometries.

What do our customers' design trends mean for Synopsys investors? As our customers retool with Synopsys' newest generation of products, our business improves. After the last several years of unimpressive growth for the EDA industry, we believe that the industry in general and Synopsys in particular will experience increased growth as a result of this retooling cycle.

Great products

Fiscal 2000 marked a turning point for Synopsys. All of our major products made good progress, but our newest product line—physical synthesis—hit the market with a force that left the competition far behind.

In the last decade, we grew from a start-up with one highly successful product, Design Compiler, into a mature company with a well-balanced portfolio of products. In 2000, we streamlined our products into five categories:

- IC implementation
- Verification and test
- Intellectual property and systems
- Transistor-level design
- Professional services

Our IC implementation business includes our Design Compiler family and the new physical synthesis products, including Physical Compiler, Chip Architect and our high-level router, FlexRoute. This is our core business line in which we have the leading market share.

Our physical synthesis products had an impressive start. For the year, these products finished at $57 million in orders—well over our aggressive initial target of $50 million. We ended the year with 71 physical synthesis customers, 18 of whom ordered

more than a million dollars' worth of product. As we go to press, we already know of over 70 tape-outs that were completed with our physical synthesis products.

Our verification and test business includes all our simulation, timing analysis, formal verification and test products. For the year, verification and test orders grew at a higher rate than overall corporate orders growth. Demand for verification products continues to increase as both systems and semiconductor companies experience a crisis in verification.

VCS, our Verilog simulator, has become the simulator of choice with the most demanding customers. Our timing product, PrimeTime, has over 80 percent market share.

Test is also doing well. With about 65 percent market share, we won additional endorsements from NEC, STMicroelectronics and Toshiba for one of our major test products this year.

Our intellectual property (IP) and system-level products include DesignWare,® models and systems design products. In our IP and systems area, we continue to lead the market in IP libraries and models. There is considerable momentum in our IP business. Few people realize that a full 30 percent of all logic chips, from those in sewing machines to satellites, contain Synopsys IP, and this area will continue to be strong for us in the future.

Our transistor-level tools include the simulation and analysis tools that we obtained through our acquisition of EPIC Design Technology in 1997. Revenue in this area declined from last year, which impacted our overall company results. However, we have had some recent wins and endorsements by key customers, and we believe that their need for the technology embedded in these tools will increase.

Our services segment includes all of our consulting and turnkey design services, training activities, and our Internet Design Services business. The fastest-growing segments of our professional services business are turnkey design, wireless and broadband products and services. We have excellent repeat business rates, mainly due to high customer satisfaction ratings. In fact, our most recent statistics show that 80 percent of our customers rated themselves as either "very" or "extremely satisfied."

Business model
In fiscal 2000, after 30 years of our industry using a perpetual license model, where the customer pays once for a long-term license, we migrated to a subscription license model for approximately 75 percent of our product orders. In this new model, the customer pays to use our software for a finite period of time, usually three years. We recognize revenue on a ratable basis over the duration of the contract, which provides us with better revenue predictability and a stronger negotiating position with customers, leading to better pricing.

Management team
In fiscal 2000, we strengthened our management team. We promoted five general managers and the head of Application Services to the corporate executive staff to increase the visibility of the product lines and their field support. We significantly strengthened the sales and finance management teams in time to execute a smooth transition to our new ratable business model. In addition, we focused one of our top executives on the creation of an Internet-based business and our CTO on building the research and IT infrastructure that will carry us beyond the billion-dollar mark. Entering fiscal 2001, we have a team in place that is ready and motivated to take Synopsys through its next stage of growth.

Field organization
We reorganized our field operations during fiscal 2000 to more effectively serve our customers. Account management was stratified into global, strategic and territory accounts. Then, along with the applications consulting teams, the accounts were more closely aligned with regional offices to provide optimal support to our customer base.

Our record bookings in fiscal 2000 illustrate the effectiveness of our focused and productive field organization. Significantly more business was generated from new customers—220 new accounts, to be exact.

Customer relationships
Synopsys takes its customer relationships seriously. This is exhibited in a number of ways. With over 65 worldwide offices, we stay in close proximity to our customers, and we pride ourselves on employing a dedicated and highly technical field force. For our global and strategic accounts, we have an executive sponsor program that dedicates one of our executives to the success of each of our key customers.

Objective measures are the best gauge of how we are doing. Last year, *EE Times*, one of the largest trade publications covering electronic design, conducted a vendor effectiveness survey of their readers. In most business-related categories, Synopsys ranked #1, including the following key categories:

- Technology Leader Today
- Technology Leader in 3 Years
- Well-Managed Company
- Clear Vision of the Future

From a customer support perspective, Synopsys ranked #1 in these categories:

- Knowledgeable Sales Reps
- Best Before-Sales Support
- Best After-Sales Support

We are proud of these results and determined to maintain them in the future.

Environment of innovation
Technology is part of Synopsys' DNA and will continue to be a key driver for us. Continuous improvement is the norm—in run-time, features and quality of results. Our patent activity is strong, and we maintain a presence through technical papers featured at major industry conferences. Let's look at just a few of the innovations that came out of the Synopsys R&D work force of over a thousand engineers this year:

- Synthesis incorporated automated chip synthesis and a new, fast HDL compiler
- Physical synthesis technology continued to improve, and we put a full routing effort in place
- VCS prepared to release the fastest Verilog gate-level simulator on the market
- Our Scirocco product was released and took the position of fastest VHDL simulator
- The award-winning TetraMax™ became the undisputed best-in-class automatic test pattern generator (ATPG)
- The SystemC-based CoCentric™ System Studio significantly widened COSSAP®'s scope of design style

Beyond EDA, we leveraged Internet technology in a revolutionary way. Today, we already have designers designing real chips over the Internet using our DesignSphere℠ environment.

These are only a few examples, but they make the point that technology is at the heart of Synopsys.

Community concerns
The Company as a whole is strong, not only in its products and financial model, but also in its spirit. Participation in the community around us is unquestionably part of what defines Synopsys. In fiscal 2000 we focused our community emphasis on supporting project-based education. Particularly rewarding was the success of the Santa Clara County science fair efforts by the Synopsys Silicon Valley Science and Technology Outreach Foundation. In one year, the number of high school students participating in local science fairs increased 400 percent, from about 200 in 1999, before we were involved, to over 1,200 in 2000.

Our involvement in the community is broader, however, than education. By participating in activities and programs that provide health and social services, promote the arts and improve the environment, the motto is always the same: Synopsys cares.

Employee concerns
As with most established high-tech companies, turnover in fiscal 2000 was higher than in past years. Our efforts to attract and hire excellent talent however, were quite successful. We are proud of the employee team that we have assembled here at Synopsys and believe that we are well positioned to take on the challenges for 2001 and beyond. Our senior management team understands that our employees are indeed the Company's most valued resource, and we are committed to providing the right work environment, tools, challenges, training, learning and growth opportunities to assure a successful and rewarding future.

In closing
This past year has been one of profound change for Synopsys and the entire EDA industry. Our customers have moved to significantly more complex designs at 0.18 micron. This is leading to a wave of retooling. The potential for growth comes as a result of this retooling wave. With physical synthesis, Synopsys has exactly the right technology at exactly the right time.

With the move to ratable licenses, we have also completed the transition to a business model that is more flexible for our customers, more balanced from a negotiation perspective and more predictable for our shareholders. The financial community already views this new model as best in class, and it is setting the direction for the entire software industry.

With few exceptions, all of our businesses are very promising, our business pipeline is strong and our industry as a whole is poised for faster growth than it has seen for the last three to four years.

Thank you for your support during this exciting journey towards future growth.

Dr. Chi-Foon Chan
President and Chief Operating Officer

Dr. Aart J. de Geus
Chairman and Chief Executive Officer

Financial pro forma performance summary[1]

(in thousands, except per share and percentage change data)
(unaudited)

	Year Ended Oct. 31, 2000[2]	Years Ended Sept. 30, 1999	1998[3]
Revenue	$ 783,778	$ 806,098	$ 661,552
Year to year percentage change[4]	(2.8%)	21.8%	14.4%
Operating margin	$ 122,014	$ 243,478	$ 161,496
Percentage of revenue	15.6%	30.2%	24.4%
Net income	$ 112,344	$ 190,736	$ 122,957
Percentage of revenue	14.3%	23.7%	18.6%
Proforma earnings per share before amortization of intangible assets			
Basic	$ 1.64	$ 2.72	$ 1.85
Diluted	$ 1.58	$ 2.60	$ 1.77
Year to year percentage change	(39.2%)	46.9%	27.3%
Cash and short-term investments	$ 435,639	$ 704,185	$ 604,630
Cash and short-term investments per diluted share[5]	$ 6.14	$ 9.59	$ 8.70
Days sales outstanding	99	61	59

[1] The Financial Pro Forma Performance Summary information excludes merger-related and other costs, in-process research and development, extraordinary items and amortization of intangible assets. Net income as presented in the Company's Consolidated Statements of Income under Generally Accepted Accounting Principles was $97.8 million, $161.4 million and $89.4 million, for the years ended October 31, 2000, September 30, 1999 and 1998, respectively.

[2] On July 15, 1999, the Board of Directors changed the Company's fiscal year to end on the Saturday nearest to October 31. Information for the October 1999 transition period was filed with Synopsys' quarterly report on Form 10-Q for the first quarter of fiscal 2000.

[3] Amounts and per share data for the periods presented in the Financial Pro Forma Performance Summary have been retroactively restated to reflect the merger with Everest Design Automation, Inc. in fiscal 1998, which was accounted for as a pooling-of-interests. Amounts also exclude the results of the PCB/Systems business of Viewlogic Systems, Inc. which was divested in fiscal 1998.

[4] The decrease in revenue in fiscal 2000 was primarily attributable to the change in the Company's new license strategy introduced in Q400. Under the new subscription strategy, relatively little revenue is recognized during the quarter the license is shipped, and the rest goes into deferred revenue to be recognized over the term of the license arrangement. Under the old form of time-based license sold in prior periods, generally all license revenue was recognized in the quarter it was shipped.

[5] On July 31, 2000, the Company announced that its Board of Directors authorized a stock repurchase program under which Synopsys common stock with a market value of up to $500 million may be acquired in the open market. The stock repurchase program replaced all prior repurchase programs authorized by the Board. During fiscal 2000, the Company purchased 9,931,500 shares at an average price of $40.02 per share, for a total amount of $397.5 million.

Readers are referred to the Company's Annual Report on Form 10-K for a complete set of financial statements as filed with the Securities and Exchange Commission.

Condensed consolidated balance sheets

(in thousands)

	Oct. 31, 2000	Oct. 31, 1999[1]	Sept. 30, 1999
Assets			
Current assets:			
Cash and cash equivalents	$ 153,120	$ 309,394	$ 285,314
Short-term investments	282,519	399,995	418,871
Accounts receivable, net	146,449	130,253	155,885
Prepaid expenses, deferred taxes and other	102,433	66,814	54,663
Total current assets	684,521	906,456	914,733
Property and equipment, net	157,243	135,118	126,204
Long-term investments	126,741	57,651	53,277
Intangible assets, net	51,776	56,240	57,393
Other assets	30,712	22,818	22,311
Total assets	$ 1,050,993	$ 1,178,283	$ 1,173,918
Liabilities and stockholders' equity			
Current liabilities:			
Accounts payable and accrued liabilities	$ 139,290	$ 98,976	$ 118,595
Current portion of long-term debt	6,416	8,658	8,610
Accrued income taxes	56,304	50,146	50,036
Deferred revenue	150,654	126,758	110,285
Total current liabilities	352,664	284,538	287,526
Long-term debt	564	11,304	11,642
Deferred compensation	14,936	9,844	9,154
Stockholders' equity:			
Capital stock	559,345	542,760	531,231
Retained earnings	405,419	349,192	371,395
Treasury stock, at cost	(329,493)	(28,589)	(43,657)
Accumulated other comprehensive income	47,558	9,234	6,627
Total stockholders' equity	682,829	872,597	865,596
Total liabilities and stockholders' equity	$ 1,050,993	$ 1,178,283	$ 1,173,918

[1] On July 15, 1999, the Board of Directors changed the Company's fiscal year to end on the Saturday nearest to October 31. Information for the October 1999 transition period was filed with Synopsys' quarterly report on Form 10-Q for the first quarter of fiscal 2000.

The financial information contained in this condensed consolidated financial statement does not constitute a complete set of financial statements. The Company's financial statements are included in the Company's Annual Report on Form 10-K filed with the Securities and Exchange Commission.

Consolidated statements of income

(in thousands, except per share data)

	Year ended Oct. 31, 2000	One month ended Oct. 31, 1999[1]	Years ended Sept. 30, 1999	1998[2]
Revenue	$ 783,778	$ 23,182	$ 806,098	$ 717,940
Expenses:				
Cost of revenue	124,474	7,380	106,764	93,767
Research and development	189,280	17,156	167,085	156,663
Sales and marketing	288,762	19,023	241,639	245,376
General and administrative	59,248	5,690	47,132	47,179
Amortization of intangible assets	15,129	1,153	7,907	--
Merger-related and other costs	--	--	--	51,009
In-process research and development	1,750	--	21,176	33,069
Total expenses	678,643	50,402	591,703	627,063
Operating margin	105,135	(27,220)	214,395	90,877
Other income, net	40,803	1,740	37,016	25,984
Income (loss) before provision (benefit) for income taxes and extraordinary items	145,938	(25,480)	251,411	116,861
Provision (benefit) for income taxes	48,160	(9,937)	90,049	55,819
Income (loss) before extraordinary items	97,778	(15,543)	161,362	61,042
Extraordinary items–sale of business unit and gain on extinguishment of debt, net of income tax expense	--	--	--	28,404
Net income (loss)	$ 97,778	$ (15,543)	$ 161,362	$ 89,446
Basic earnings per share:				
Income (loss) before extraordinary items	$ 1.43	$ (0.22)	$ 2.30	$ 0.92
Extraordinary items	--	--	--	0.42
Net income (loss)	$ 1.43	$ (0.22)	$ 2.30	$ 1.34
Weighted average common shares	68,510	70,400	70,118	66,568
Diluted earnings per share:				
Income (loss) before extraordinary items	$ 1.38	$ (0.22)	$ 2.20	$ 0.88
Extraordinary items	--	--	--	0.41
Net income (loss)	$ 1.38	$ (0.22)	$ 2.20	$ 1.29
Weighted average common shares and equivalents	70,998	70,400	73,422	69,524

[1] On July 15, 1999, the Board of Directors changed the Company's fiscal year to end on the Saturday nearest to October 31. Information for the October 1999 transition period was filed with Synopsys' quarterly report on Form 10-Q for the first quarter of fiscal 2000.

[2] Amounts and per share data for the periods presented have been retroactively restated to reflect the merger with Everest Design Automation, Inc. in fiscal 1998, which was accounted for as a pooling-of-interests.

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Pro forma consolidated statements of income[1]

(in thousands, except per share data)
(unaudited)

	Year ended Oct. 31, 2000	One month ended Oct. 31, 1999[2]	Years ended Sept. 30, 1999	1998[3]
Revenue	$ 783,778	$ 23,182	$ 806,098	$ 661,552
Expenses:				
Cost of revenue	124,474	7,380	106,764	84,095
Research and development	189,280	17,156	167,085	145,750
Sales and marketing	288,762	19,023	241,639	227,047
General and administrative	59,248	5,690	47,132	43,164
Total expenses	661,764	49,249	562,620	500,056
Operating margin	122,014	(26,067)	243,478	161,496
Other income, net	40,803	1,740	37,016	25,984
Income (loss) before provision (benefit) for income taxes and extraordinary items	162,817	(24,327)	280,494	187,460
Provision (benefit) for income taxes	50,473	(7,785)	89,758	64,503
Net income (loss)	$ 112,344	$ (16,542)	$ 190,736	$ 122,957
Basic net income (loss) per share	$ 1.64	$ (0.23)	$ 2.72	$ 1.85
Weighted average common shares	68,510	70,400	70,118	66,568
Diluted net income (loss) per share	$ 1.58	$ (0.23)	$ 2.60	$ 1.77
Weighted average common shares and equivalents	70,998	70,400	73,422	69,524

[1] The Pro Forma Consolidated Statements of Income information excludes merger-related and other costs, in-process research and development, extraordinary items and amortization of intangible assets. Net income as presented in the Company's consolidated statements of income under Generally Accepted Accounting Principles was $97.8 million, $161.4 million and $89.4 million, for years ended October 31, 2000 and September 30, 1999 and 1998, respectively.

[2] On July 15, 1999, the Board of Directors changed the Company's fiscal year to end on the Saturday nearest to October 31. Information for the October 1999 transition period was filed with Synopsys' quarterly report on Form 10-Q for the first quarter of fiscal 2000.

[3] Amounts and per share data for the periods presented have been retroactively restated to reflect the merger with Everest Design Automation, Inc. in fiscal 1998, which was accounted for as a pooling-of-interests. Amounts exclude the results of the PCB/Systems business of Viewlogic systems, Inc., which was divested in fiscal 1998, merger-related and other costs, in-process research and development, extraordinary items and amortization of intangible assets.

Executive officers

Aart J. de Geus, Ph.D
Chief Executive Officer and Chairman of the Board

Chi-Foon Chan, Ph.D
President and Chief Operating Officer

Vicki L. Andrews
Sr. Vice President, Worldwide Sales

David P. Burow
Sr. Vice President and General Manager, Internet Design and Services Group

Raul Camposano, Ph.D
Chief Technology Officer

John Chilton
Sr. Vice President and General Manager, Intellectual Property and Systems Group

Antun Domic, Ph.D
Sr. Vice President and General Manager, Nanometer Analysis and Test

Manoj Gandhi
Sr. Vice President and General Manager, Verification Technology Group

Deirdre Hanford
Sr. Vice President, Business and Market Development

Robert B. Henske
Sr. Vice President, Finance and Operations, Chief Financial Officer and Treasurer

Ernst W. Hirt
Sr. Vice President, Human Resources and Facilities

Scott Houghton
Sr. Vice President and General Manager, Synopsys Professional Services

Sanjiv Kaul
Sr. Vice President and General Manager, Physical Synthesis Group

Steven K. Shevick
Vice President, Investor Relations and Legal, General Counsel and Corporate Secretary

Jack Warecki
Sr. Vice President, Worldwide Application Services

Board of directors

Aart J. de Geus, Ph.D
Chief Executive Officer and Chairman of the Board

Chi-Foon Chan, Ph.D
President and Chief Operating Officer

Andy D. Bryant
Director

Deborah A. Coleman
Director

Harvey C. Jones, Jr.
Director

William W. Lattin, Ph.D
Director

A. Richard Newton, Ph.D
Director

Sasson Somekh, Ph.D
Director

Steven C. Walske
Director

Corporate information

Transfer Agent & Registrar:
Computershare Investor Services
2 North LaSalle Street
Chicago, IL 60602

Form 10-K
If you would like to receive, without charge, a copy of the Company's Form 10-K as filed with the Securities and Exchange Commission, or would like to receive other stockholder communications, please send your request to:

Investor Relations
Synopsys, Inc.
700 East Middlefield Road
Mountain View, CA 94043
650-584-4257

Annual meeting
April 6, 2001

Corporate headquarters

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700 East Middlefield Road
Mountain View, CA 94043
650-584-5000

International headquarters

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Blanchardstown Corporate Park
Blanchardstown
Dublin 15, Ireland
353-1-808-9180

Regional headquarters

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