Renu Mehra

Group Director, R&D, Silicon Realization Group

Renu Mehra is R&D Group Director for the Silicon Realization Group at Synopsys and heads the Design Compiler® R&D Team. During her time at Synopsys, she has led teams that have delivered several advanced technologies including RTL synthesis and optimization, clock gating, constraint management, multi-voltage designs, power management approaches, and congestion, power, and runtime optimizations. Extending her influence beyond her team, Renu actively works with product groups across Synopsys, leads the cross-business-unit power management initiative, and works with various functional groups including applications engineering, marketing, field engineers, sales, and product validation.

Renu is a pioneer in design automation for power management and provided one of the early visions for an automated solution for this area. Her Ph.D. work in low-power technologies helped enable a computational tablet featuring capabilities like speech and handwriting recognition, prior to the advent of today's consumer tablets. As one of the founding members of the IEEE 1801 working group that created the Unified Power Format, she had the opportunity to shape what is now the dominant power intent specification format for the semiconductor industry. Renu earned a bachelor's degree in Electrical Engineering from the Indian Institute of Technology, Kanpur, and an M.S. and Ph.D. in Electrical Engineering and Computer Sciences, respectively, from the University of California, Berkeley. She has three U.S. patents awarded and two patents filed. Renu considers the ability to work on technically challenging problems and to see the results being deployed in real customer designs to be among the most rewarding aspects of her work.