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Janick Bergeron is a Fellow at Synopsys. He is the author of the best-selling Verification Methodology Manual for SystemVerilog and Writing Testbenches: Functional Verification of HDL Models. He is also the founder and moderator of the Verification Guild forum and writes the verification methodology blog Verification Martial Arts.

Prior to joining Synopsys, Mr. Bergeron worked on verification methodology at Qualis Design Corporation and Bell-Northern Research.

Mr. Bergeron holds a Master degree in Electrical Engineering from the University of Waterloo, a Bachelor of Science degree in Engineering from the Université du Québec, and an MBA degree granted through the University of Oregon.