Agenda

• 12:45 – 13:15: Registration

• 13:15 – 13:30: Welcome

• 13:30 – 15:00: Sessions Block S1

• 15:00 – 15:30: Break

• 15:30 – 17:00: Sessions Block S2

• 17:00 – 18:30: Social poster session
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**Social poster session**: Join us for drinks and snacks and the possibility to talk to Synopsys R&D and fellow attendees!
Registration Information

• To register, please send email to:
  
  Claudia Heidinger
  Email: heiding@synopsys.com

• Please specify which track & sessions you plan to attend, for example:
  – B1, A2, C2
• **Title:** Synopsys’ Test Point Applications Tutorial  
• **Abstract:**  
  Adding test point logic to a design can improve the testability, fix DFT DRC violations and lower the test time and test cost. Synopsys offers a number of tools and features to identify and select the test points locations for different targets, perform what-if analysis and automatically insert the test points with minimal impact on timing, power, area and congestion.

  This tutorial gives an overview of all available test point capabilities in DFT Compiler/DFTMAX, TetraMAX and SpyGlass DFT ADV and explains the test point types, the user interfaces and the flows.

• **Presenters:** Frank Nolting, Synopsys AC  
• **Schedule:** 13:30 – 14:15 Uhr  
• **Target-Audience:** DFT Engineers, Designers
Track: Implementation Platform
Session A2

• **Title:** *IC Compiler II GUI, A hands on tutorial on how to use IC Compiler II's route editor to interactively route and edit critical signals before detail route*

• **Abstract:**

The IC Compiler II Interactive Design Environment (IDE), provides a rich and powerful environment for the all phases of the physical implementation flow. Providing leading edge capabilities for Interactive Design Planning, Pre-Route and Post-Route Editing, Clock Tree Synthesis, Timing Analysis, UPF/Power, Test, Chip Finishing, and in-design integration with the signoff tools.

As chips are becoming more and more complex there is a need to achieve much higher performance on critical signals & busses to differentiate your products vs. competition. These are connections that need to me made prior to detail routing. IC Compiler II has a rich set of route editing features for creating, editing, and debugging of these critical signals. We will explore how to use Create Rout Tool (CRT) to connect full custom signals, groups of nets, bundles and how to shield the bundles. We will also look at some of the key features to help the user debug during this critical routing phase. Finally we will cover some advanced features of Route editing environment such as Multi-Level Physical Hierarchy support, how to achieve self-healing routes. After this tutorial you will have the background you need to start boosting your productivity by interactively using ICCII route editor.

• **Presenters:** Dan Guilin, Synopsys R&D

• **Schedule:** 14:15 – 15:00 Uhr

• **Target-Audience:** Physical Designers
Track: Implementation Platform
Session A3

• **Title:** Synopsys Digital Implementation Technologies to Meet Aggressive QoR and TAT Goals for Established and Emerging Node Designs

• **Abstract:**

Design teams implementing high performance, low power designs are facing new challenges to meet their performance targets with extremely tight design schedules. In addition, advanced node rule formulations require dedicated implementation features to achieve optimal power, performance and area in a full RTL to Signoff digital design implementation flow.

In this presentation, we will cover new capabilities and innovative core technologies in Design Compiler Graphical, IC Compiler II and Primetime to deliver comprehensive solutions to designers implementing both emerging and established node designs across a multitude of applications and process technology nodes. This tutorial presents key design implementation techniques and delivers an under the hood look at Synopsys’ Digital Design Implementation and Signoff tools to achieve aggressive timing performance, lowest leakage and dynamic power, best in class area and fastest runtime. After attending this tutorial, attendees will have a good understanding of Synopsys’ latest digital design implementation technology offerings and will be able to deploy them in their production design flows.

• **Presenters:** Thomas Andersen, Synopsys R&D

• **Schedule:** 15:30 – 17:00 Uhr

• **Target-Audience:** Logical and Physical Designer Manager
Track: Best Practice
Session B1

• Title: Debugging and Resolving Failing and Inconclusive Verifications in Formality

• Abstract:

When a verification run reports that the designs are not equivalent, failure is due either to an incorrect setup or to a logical design difference between the two designs. Moreover, occasionally, Formality encounters a design that cannot be verified because it is particularly complex. The session provides information about the frequently used tools and strategies in Formality and Formality Ultra that assist users in debugging failing or hard verifications, improving designer productivity and accelerating the time to successful verification also in case of most complex and highly optimized designs.

• Presenters: Dr. Manuela Anton, Synopsys AC

• Schedule: 13:30 – 14:15 Uhr

• Target-Audience: Logic Design & Verification Engineers
Track: Best Practice
Session B2

• Title: *Introduction to Reset Domain Crossing Analysis with SpyGlass RDC*

• Abstract:
Reset Domain Crossings (RDCs) have the same devastating consequences as Clock Domain Crossings (CDCs) causing functional failure due to Metastability. RDC particularly impacts design functionality during initialization and it is now emerging as one of the leading cause of chip failure for design with multiple power domains where various power domains are switched on and off for power saving purposes.

This session covers fundamental problems with Reset Domain Crossings and the three design architectural choices commonly used to prevent Metastability across reset domains. We will then present a simple methodology to verify and eradicate RDC hazards using SpyGlass RDC.

• **Presenters:** James Gillespie, Synopsys CAE
• **Schedule:** 14:15 – 15:00 Uhr
• **Target-Audience:** Verification & Implementation Designer
**Track: Best Practice**

**Session B3**

- **Title:** *Boosting Debug Productivity with Verdi – Practical Applications of Debug Innovations*

- **Abstract:**
  
  With the growing complexity of today’s SoCs, teams are facing intense time pressures for SoC verification closure, with engineers on the lookout for better verification and debug methodologies. As verification teams migrate to SystemVerilog and UVM class-based testbenches for higher efficiency and increased verification reuse across projects, debug methodology needs to scale accordingly to fully realize the benefits of this migration.

  In this best practice session, we will focus on practical applications of Verdi debug innovations:
  
  - Root causing a complex testbench bug with SVTB/UVM-aware Reverse Debug natively integrated with simulation
  - Novel techniques to speed up SoC exploration and debug using OneSearch
  - Faster fully integrated debug at all SoC levels, from design to embedded SW

  Attendees will take home an arsenal of techniques they can put to immediate use to significantly boost their debug productivity.

- **Presenters:** Joerg Richter, Synopsys R&D

- **Schedule:** 15:30 – 17:00 Uhr

- **Target-Audience:** Digital Verification Engineers
Title: Mixed Signal Verification of UPF based designs

Abstract:

Due, in a large part, to the huge demand for mobile devices, reducing the power consumption of microchips is one of the most important goals in electronic design today. In order to reduce the amount of power demanded by these chips, engineers are architecting increasingly complex power supply schemes.

These systems now have many power modes that enable sections of the design to be either turned off completely or driven to different supply voltages. These separate power islands (known as power domains) each need their own power switches, as well as the supporting structures e.g. level shifters, retention and isolation circuitry, to ensure that corrupt data does not cause a functional failure of the system. Implementing and then verifying this power supply logic is now a significant consideration in the design of modern chips.

Unified Power Format (UPF) is a standard format (IEEE-1801) that allows the power supply strategy of a system on chip to be defined. This UPF file is then used within both the implementation and verifications flows, to ensure that this power intent is followed. The majority of electronic systems contain some analog circuitry e.g. on chip voltage regulators that provide the supplies for the rest of the chip. It is therefore important to verify the functionality of these analog macros in the context of the overall system.

This tutorial will illustrate via a practical example, how the power intent for a mixed signal UPF design containing SPICE descriptions of the voltage regulators and analog macros can be verified using a UPF driven simulation approach. The example walks though the UPF creation, simulation and debug for a sigma-delta ADC. Recommendations are made as to how the UPF for the analog blocks can be structured to ensure that the same UPF can be used for implementation and verification of the System. The example also illustrates some of the potential design issues both in the analog design and in the overall system, that can be identified using this methodology.

Presenters: Damian Roberts, Synopsys AC

Schedule: 13:30 – 15:00 Uhr

Target-Audience: Mixed-Signal Verification and CAD Engineers/Managers
Title: *A Practical Guide to SystemVerilog Nettype (Real) Number Modelling in Mixed Signal Simulation (VCS AMS) with advanced Analog Mixed Signal Debug (Verdi AMS) while utilizing re-usable SystemVerilog Testbenches.*

**Abstract:**

In this tutorial users will learn how to incorporate SystemVerilog Nettype (Real) Number models into Synopsys’s Premier Mixed Signal Simulation tool (VCS AMS) for high performance Mixed Signal Verification.

Re-usable SystemVerilog Testbenches incorporating Cross Module references force/release and read will be utilized for interchangeable Analog (Spice) and Digital targets.

Users will learn how to use, from SystemVerilog, XMRs (Cross Module References) Reads, Forces and Releases on Nettypes (Real) Arrays of Nettype (Real) and SPICE bus formats.

Advanced interactive and batch Mixed Signal Simulation and Debug will be performed with VCS AMS and Verdi AMS and Synopsys’s Custom Waveview high performance Analog Waveform tools, users will learn how to debug static and dynamic (Power Supply Dependent) auto inserted Analog/Digital interface converters for nettypes, review their placement and optimize performance.

**Presenters:** Peter Thompson, Synopsys CAE

**Schedule:** 15:30 – 17:00 Uhr

**Target-Audience:** Mixed-Signal Verification and CAD Engineers/Managers
SNUG Germany 2017
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SNUG Germany – 29th June, 2017
Munich City Hilton Hotel

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