



ARC EM SEP Starter Kit User Guide

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This chapter outlines the document structure and provides a brief chapter overview. Additionally, it contains a list of available resources and other supporting documents.

Document Structure

This document consists of the following chapters:

- [Preface](#) – Overview of the available documentation and its organization.
- Introduction – Overview of the ARC EM SEP, target applications, and the tool requirements.
- Working with ARC EM SEP on the Starter Kit Board – Procedures for configuring ARC EM SEP.
- ARC EM SEP Configuration – Information about the ARC EM SEP configuration.
- Mapping the ARC EM SEP FPGA Image – Information about the actions to program the ARC EM Starter Kit board.
- Glossary and References – List of abbreviations, terms, and external references.

This document describes the ARC EM Safety Enhancement Package Starter Kit.

Refer to the ARC EM Starter Kit User Guide for a detailed description of the board hardware, its peripherals, software and tools required and to the DesignWare ARC EM SEP Databook for a detailed description of the ARC EM SEP processor family.

About the ARC EM SEP Image

The ARC EM SEP configuration supplied is an FPGA image used with the ARC EM Starter Kit hardware platform.

The configuration provided is based on the **EM4_Parity** template. This template has following main parameters:

- 32-bit address space with parity protection (data only) on ICCM0 and DCCM
- 24-bit program counter (PC) and 8-bit loop counter (LC) registers
- 16 core registers

The FPGA image of ARC EM SEP has additional features:

- ICCM0 size is increased to 128 KB
- DCCM size is increased to 64 KB
- Divider option is Radix2
- Multiplier option is wlh5
- Actionpoints
- SmaRT
- Timers
- On-board peripherals

Comparing ARC EM SEP with the default configurations of ARC EM Starter Kit the main differences are:

- ICCM0 and DCCM sizes
- ICCM0 and DCCM have parity protection bits
- No external memory controller (DDR3)
- No DSP block

- Divider and multiplier are added
- CPU reset state is halt
- 24-bit program counter (PC) and 8-bit loop counter (LC) registers
- 16 core registers

The ARC EM SEP FPGA image is provided with the ARC EM Starter Kit development board. The board is based on a Xilinx Spartan®-6 LX150 FPGA and it supports hardware extensions using six 2x6 connectors supporting a total of 48 user I/O pins (plus power and ground pins) that can be used to connect components such as sensors, actuators, memories, displays, buttons, switches, and communication devices. A Digilent Pmod™ compatible extension board containing a four-channel 12-bit A/D converter with an I2C interface and an AC power adapter is included in the package.

Target Applications

The ARC EM SEP processor series is designed for use in embedded safety applications where the highest level of safety integrity is required. ARC EM SEP processors are based on the ARC EM architecture, which provides high performance with minimum power consumption.

You can connect the following end-devices to the ARC EM Starter Kit:

- Sensors
- Actuators
- Displays
- Buttons
- Switches
- Communication devices

Tool Requirements

The ARC EM SEP Starter Kit requires the following tools to be installed on your host:

- Digilent Adept software — Software driver for the Digilent JTAG-USB cable.
- Xilinx iMPACT tool — Software tool to program an FPGA image on the ARC EM Starter Kit board.
- MetaWare Development Toolkit — DesignWare ARC tools to run and debug applications on DesignWare ARC processors.

Working with ARC EM SEP on the Starter Kit Board

This chapter describes the on-board devices, human-machine interface, and power supply used with the ARC EM SEP Starter Kit.

On-Board Devices

JTAG Connector

It is best to use the USB interface for JTAG debugging. Alternatively, it is possible to use industry-standard debug probes connected to the 20-pin JTAG connector J15.

The ARC EM Starter Kit supports a standard four-wire JTAG interface. The two-wire IEEE 1149.7 C JTAG is not supported.

USB

The mini-USB port can be used for several purposes:

- ARC JTAG debugging port
- UART debug console
- FPGA bitfile programming

Put jumper J8 in place for FPGA programming and remove it when the USB port is used for ARC JTAG or as a UART debug console.

SD Card

The SD card interface works in SPI mode. It is connected to channel 3 of the SPI Master.

Human-Machine Interface

The following components are available on the ARC EM Starter Kit board:

- Push buttons
- DIP-switches
- Jumpers
- LEDs

Push Buttons

Name	Location	Description
A	Above letter 'A' of the ARC logo	ARC start button when processor is halted. This button is also connected to DW GPIO Port A[2]. Debouncing is implemented inside the DW GPIO IP. Note that when the processor is halted (for example, for debugging), pressing this button continues execution. Pay special attention to this button in debug mode; in general mode it may be used by the user application same way as the 'L' and 'R' buttons.
Reset	Above letter 'R' of the ARC logo	ARC reset.
C	Above letter 'C' of the ARC logo	Configure button. Pushing this button has the same effect as a power-on reset and triggers the FPGA to re-load the bitfile from the serial flash memory.
L	Marked 'L'	User button. This button is connected to DW GPIO Port A[0]. Debouncing is implemented inside the GPIO IP.
R	Marked 'R'	User button. This button is connected to DW GPIO Port A[1]. Debouncing is implemented inside the GPIO IP.

Note: Three push buttons (A, L, R) are available for user purposes.

DIP-Switches

The four-bit DIP-switch SW1 is used for controlling input ports for user GPIOs.

- Switch 1 is connected to GPIO Port C[0].
- Switch 2 is connected to GPIO Port C[1].
- Switch 3 is connected to GPIO Port C[2].
- Switch 4 is connected to GPIO Port C[3].

Jumpers

Refer to *ARC EM Starter Kit Getting Started* for more information.

LEDs

Nine LEDs can be used as output ports for user GPIOs. LEDs 0 to 8 are located below the ARC Synopsys logo on the board. LED8 is located next to DIP switch SW1.

LED GPIO mapping:

- GPIO Port B[0] controls LED0
- GPIO Port B[1] controls LED1

- ...
- GPIO Port B[8] controls LED8

If the LED is on, its corresponding control bit is programmed to 0.

Power Supply

Use the universal power adapter (110-240 Volts AC to 5 Volts DC) from the package.

1. Connect the appropriate AC plug for your AC power outlet.
2. Connect the DC plug to the connector J13 “5V DC” on the board.
3. Connect the AC plug to your AC power outlet.

ARC EM SEP Configuration

This chapter is intended for programmers of the ARC EM SEP.

Programmer's Model

The ARC EM SEP provides an **EM4_Parity** core configuration that can be used for running applications on a 30 MHz CPU clock.

The detailed configuration is described in [Detailed Core Configuration](#).

Core Configuration and Memory Mapping

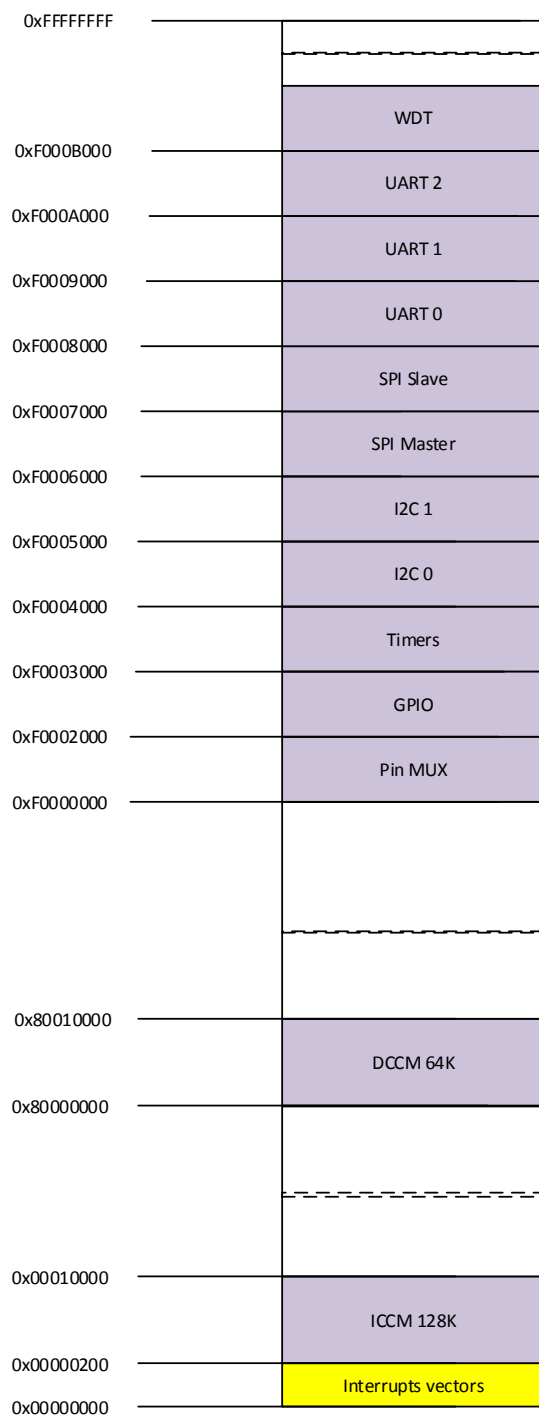
From a programmer's point of view, the ARC EM SEP provides a memory map of ARC EM4. ARC EM4 is an ARC EM core with 32 bits of address space, 128 KB of code memory (ICCM), and 64 KB of data memory (DCCM).

The MetaWare compiler options for this configuration are:

```
-arcv2em -core1 -rf16 -HL -Hlpc_width=8 -Hpc_width=24  
-Xcode_density -Xdiv_rem=radix2 -Xswap -Xnorm -Xmpy16 -Xmpy -Xmpy  
_cycles=5 -Xshift_assist -Xbarrel_shifter -Xtimer0 -Xtimer1
```

The memory map is shown in [Figure 1](#).

Figure 1 Memory Map of ARC_EM4 Configuration



Detailed Core Configuration

Table 1 Configuration Details

Configuration Option	Description	ARC_EM4_SEP
iccm0_prot	Protection from data errors in memory.	Parity
iccm0_prot_level	The level protection from errors in core	Data_Only
iccm0_prot_exceptions	Builds exception hardware for uncorrectable data errors read from the ICCM	true
dccm_prot	Specifies the protection from errors in the core.	Parity
dccm_prot_level	The level protection from errors in core	Data_Only
dccm_prot_exceptions	Builds exception hardware for uncorrectable data errors read from the DCCM	true
addr_size	Address width.	32
pc_size	PC width.	24
lpc_size	Loop counter width.	8
code_density_option	Code Density ISA extension.	true
bitscan_option	Bit-Scan ISA extension.	true
number_of_interrupts	Highest valid interrupt number.	9
external_interrupts	Number of external interrupt pins.	7
intvbase_preset	Interrupt vector base.	0
rgf_num_regs	Number of core registers.	32
rgf_wr_ports	Register file: number of write ports.	1
byte_order	Endianness.	little
shift_option	Shift option.	3
swap_option	SWAP instruction.	true
div_rem_option	DIV/REM option.	radix2
mpy_option	Multiplier ISA option.	wlh5
timer_0_int_level	Timer 0 interrupt level.	1
timer_1_int_level	Timer 1 interrupt level.	0
dccm_size	Size of the Data Closely Coupled Memory (DCCM) in bytes.	65536

Configuration Option	Description	ARC_EM4_SEP
stack_checking	Include logic for validating stack accesses. Stack access violations are subject to privilege violation exceptions.	false
code_protection	Disables any load or store to the corresponding region.	false
dccm_dmi	DCCM has DMI port.	false
iccm0_size	Defines the size of ICCM0 in bytes. This ICCM has 0 wait states.	131072
iccm0_base	Sets the initial memory region assignment for ICCM0.	0
iccm0_dmi	ICCM0 has DMI port.	false
rgf_num_banks	Two register banks are needed for fast IRQ, but may be selected even without.	1
rgf_banked_regs	Number of banked registers.	32
number_of_levels	Number of interrupt levels.	2
firq_option	Fast IRQ enabled.	false
num_actionpoints	Number of trigger events available.	2
aps_feature	Selects Actionpoint feature set.	min
smart_stack_entries	Specifies the number of entries in the trace buffer.	8

Troubleshooting

The following message may appear when you try to connect using the MetaWare debugger

```
[DIGILENT] Device enumeration: #0 is `TE0604-02'=JTAG-ONB4.
[DIGILENT] We choose device : #0 `TE0604-02' from 1 possible
devices.
[DIGILENT] Product=508 variant=1 fwid=57 firmware-version=108.
[DIGILENT] It is possible to set the JTAG speed.
[DIGILENT] Current speed is 10000000 Hz.
[JTAG] ARC 1 does not exist; the chain has 0 ARCs.
Download failed (2).
No process.
Exiting due to error and because exit_on_error=1.
C:\ARC\MetaWare\arc\bin\cld: Permission denied
```

This means that the J8 jumper was left after programming the FPGA. Remove it to eliminate this message.

1. Make sure that you are using the correct console settings for the `dw_apb_uart` application:

```
Baudrate=115200 Kb/s  
Bits=8  
Parity=None  
Stop=1
```

Mapping the ARC EM SEP FPGA Image

This section describes the ways to map the ARC EM SEP FPGA image to the ARC EM Starter Kit board.

Methods for Mapping the ARC EM SEP Image

There are two methods to map the ARC EM SEP FPGA image to the Starter Kit board:

- Bitfile programming directly onto the FPGA device
- SPI Flash ROM programming

See “FPGA Image Recovery” in the *ARC EM Starter Kit User Guide* for a detailed description of software and hardware tools required for FPGA image or SPI Flash ROM programming and the actions required to perform it.

Glossary and References

This chapter contains a list of specific terms used in this document and references for further reading.

Glossary

APB

AMBA Advanced Peripheral Bus

AHB

AMBA Advanced High Performance Bus

ARC EM SEP

ARC EM Safety Enhancement Package

DCCM

Data Closely Coupled Memory

DMP

Data Memory Pipeline (ARC proprietary bus)

DW

Synopsys DesignWare IP solutions

GPIO

General Purpose Input/Output pins

ICCM

Instruction Closely Coupled Memory

Pmod

Digilent Pmod™ socket connector

References

- [1] *ARC EM Starter Kit Getting Started*
http://www.synopsys.com/dw/ipdir.php?ds=arc_em_starter_kit
- [2] *ARC EM Starter Kit User Guide*
http://www.synopsys.com/dw/ipdir.php?ds=arc_em_starter_kit
- [3] *DesignWare ARC EM SEP Databook*
<http://www.synopsys.com/dw/ipdir.php?ds=arc-em-sep>