SNUG UK 2016 · Thursday, June 30, 2016 · Hilton Reading

Don't Miss Out! SNUG UK Highlights and Special Events

- Attend the keynote by John Koeter, Vice President, Solutions Group, Synopsys
- Choose from over 25 technical presentations on advanced technologies and design styles by Users and Synopsys experts
- Network and connect with Synopsys executives and members of the local design community

8:15 - 9:00	**Registration and Breakfast**				
9:00 - 10:15	**Program Overview:** Jonathan Young, Director, Applications Consulting, Synopsys UK **Welcome and Introduction:** Mike Bartley, UK SNUG Technical Chair, Test and Verification Solutions Ltd. **Synopsys Keynote:** John Koeter, Vice President, Solutions Group, Synopsys, Inc.				
10:15 - 10:45	**Break**				
	Automotive	**Advanced Logical Implementation**	**High-Performance Implementation**	**Verification**	**Custom and Analog Mixed-Signal**
10:45 - 11:30	**Optimisation of DFTMAX Ultra Scan Patterns** Dialog Semiconductor, Dialog GmbH	**Advanced Reporting with PrimeTime** Synopsys	**Effective ICG Enable Timing Optimization Throughout the Galaxy Implementation Flow** Synopsys	**Effective SystemVerilog Functional Coverage: Design and Coding Recommendations** Verilab Ltd., Verilab GmbH	**CCK GUI Integration Flow – Custom Voltage Domain Checks to Catch Real-Life Tapeout Killers** Dialog Semiconductor
11:30 - 12:15	**Synopsys Test Solution Certified for the Most Stringent Level of Automotive Safety Measures Defined by ISO 26262 Standard** Synopsys	**Conclusive Formal Verification of Clock Domain Crossings using SpyGlass-CDC** STMicroelectronics, Synopsys	**Implementing the Complete Signoff-Ready Reference Flow for Imagination Technologies PowerVR GPU Cores using Synopsys' Next Generation Tools** Imagination Technologies	**CTAL - Clock Tree Abstraction Layer**	**Bringing Harmony to Analogue Testbenches by Utilizing Verilog-A** Dialog Semiconductor
12:15 - 13:30	**Lunch**				
13:30 - 14:15	**Build in Software Security Throughout the Automotive Supply Chain** Synopsys	**Galaxy RTL: Design Compiler Family 2016.03 Update and Best Practices for Faster Runtime on Large Designs** Synopsys	**Best Practices for High-Performance, Energy Efficient Implementations of the Latest ARM Processors in 16-nanometer FinFET Plus (16FF+) Process Technology using Synopsys Galaxy Design Platform** Synopsys	**Reusable Verification Framework** EnSilica	**Comprehensive AMS Verification Using Octave, Real Number Modelling and UVM** Xilinx
14:15 - 15:00	**Reach ASIL Targets for Automotive Designs with Ethernet QoS IP and Certified Flow** Synopsys	**The Causes and Identification of Inefficient and Redundant Clock Gating** Dialog Semiconductor		**Improving X Debug in X Prop and GLS Simulations** Imagination Technologies, Synopsys	**Incorporating System Verilog Real Number Models in Mixed Signal Simulation (VCS AMS) with Advanced Analog Mixed Signal Debug (Verdi AMS) and Utilizing Re-Usable System Verilog Testbenches** Synopsys
15:00 - 15:30	**Break**				
15:30 - 16:15	**Accelerating the Path to SoC Safety Certification (ISO 26262)** Synopsys	**Complete Low Power Verification using Formality** Synopsys	**Floorplan a Multi-Million Gate, Leading Edge, Complex Processor Cluster? You'll Have it in Less Than a Week** Imagination Technologies, Synopsys	**Formal Coverage Analysis: Concepts and Practicalities** HUAWEI Technologies	**De-Mystifying TCL Custom Application Creation in Maxwell, with Automatic AMS IP Block Documentation** Elmos Semiconductor AG, Synopsys
16:15 - 17:00	**Designing Safer Cars – A Journey in ISO 26262 Territories** Synopsys	**Functional ECO User Case Studies using Formality Ultra** Synopsys	**Floorplanning Large Blocks Using IC Compiler II** Synopsys	**Is the Glass Half Full or Half Empty? An Introduction to Synopsys Formal Coverage Analysis** Synopsys	**Learn About the Latest Innovations in Custom Design for Advance Nodes in this Technology Walk-Through** Synopsys
17:00 - 18:00	**Awards & Refreshments**				