SNUG Taiwan 2016 · September 7–8 · Ambassador Hsinchu Hotel

Don't Miss Out! SNUG Taiwan Highlights and Special Events

- Attend the opening keynote by Aart de Geus, Chairman & co-CEO, Synopsys
- Choose from over 45 technical presentations on advanced technologies and design styles by Users and Synopsys experts
- Attend the Custom Design panel to gain insights on optimal custom layout practices

DAY 1 – September 7, 2016

9:10 - 9:20	**Opening**				
9:20 - 10:00	**Synopsys Keynote Address: "Silicon to Software: Smart Everything!"** – Dr. Aart de Geus, Chairman and co-CEO, Synopsys				
10:00 - 10:40	**MediaTek Keynote Address: "MediaTek IoT: Everything Connected, Everyday Genius"** – Dr. JC Hsu, Corporate VP and GM of IoT Business Development, MediaTek				
10:40 - 11:00	**Welcome and Technical Program Overview** – SNUG Taiwan Technical Committee Chairperson, Shu-Yi Kao, Director, Realtek				
11:00 - 11:20	**Break**				
	Implementation		**Verification**	**Custom Design**	
11:20 - 12:00	**Best Practices for High-Performance, Energy Efficient Implementations of the ARM® Cortex®-A73 Processor in 16-nanometer FinFET Plus (16FF+) Process Technology Using Synopsys Galaxy™ Design Platform** ARM, Synopsys		**Synopsys Verification Overview and Direction** Synopsys	**Custom Compiler Introduction** Synopsys	
12:00 - 1:30	**Lunch**				
	Implementation		**Verification**	**Custom Design**	**Advanced Research**
1:30 - 3:30	**N20 ARM Midgard High Performance GPU Implementation – Preparing the Best Starting Point for Real Silicon** MediaTek		**Equivalence Checking for SPICE Netlist and IO Macro Model** MediaTek	**Synopsys Custom Compiler Certification for TSMC 10nm Paves the Path to 7nm** TSMC	**Modern VLSI Circuit Placement** NTU
	Improved Predictability and Quality of Results with Design Compiler Graphical GUC		**Low Power Verification for Complex IO Macro Power Relation** MediaTek	**Implement FinFET Solution in Laker and Improve Layout Productivity** Sunplus	
	Best Practices for a Performance and Area Focused Implementation of High-Performance GPUs Using Galaxy Design Platform Synopsys		**Essential Ingredients of Formal Verification** Synopsys	**Custom Layout Panel – Layout Challenge and Solution** Himax, Nuvoton, Silicon Topology, Synopsys	**Routability Estimation for Modern VLSI Design** NTHU
3:30 - 4:00	**Break**				
	Physical Implementation	**Test**	**Verification**	**Custom Design**	**Advanced Research**
4:00 - 6:00	**Mali-T400 Series Large Flatten and Hierarchical Design Implementation Flow with IC Compiler II** Novatek	**TetraMAX II for 25% Fewer Patterns and 10x Faster Runtime** Synopsys	**Advanced Simulation** Synopsys	**UMC iPDK Update and FinFET Solution** UMC	**Intelligent IoT** NCTU
	Achieving Industry Best QoR on Advanced Design with IC Compiler II Synopsys	**Hierarchical DFT on Hundreds Million Gate Design** MediaTek		**Advantage of Synopsys Layout Solution and UDD Device Upgrade** UMC	
		Diagnostics with TetraMAX for Reliability Analysis		**LakerOA Adoption Challenge and Advantage** Richtek	
	Floorplanning Large Blocks Using IC Compiler II Synopsys	**Experience Sharing on In-System Self-Test Using DFTMAX LogicBIST and SpyGlass** GUC	**Static Analysis with SpyGlass** Synopsys	**Increase Layout Productivity with Top Down Schematic Driven Layout Flow** Synopsys	**Advanced Research Panel** NTU, NTHU, NCTU, Synopsys
		Address Testability Issues Early with SpyGlass DFT ADV RTL Testability Analysis Synopsys			

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DAY 2 – September 8, 2016

9:10 - 9:20	**Opening**
9:20 - 10:00	**ARM Keynote Address: "Navigating the New Age of Connected Intelligent Products"** – John Ronco, Vice President of Product Management, CPU Group, ARM
10:00 - 10:40	**TSMC Keynote Address: "Integration of Technology – Enabling IoT"** – Dr. Simon Wang, Senior Director of Internet of Things Business Development, TSMC
10:40 - 11:00	**Best Paper Award** – SNUG Taiwan Technical Committee
11:00 - 11:20	**Break**
11:20 - 12:00	**IoT IC Design Challenges and IP Innovation** – Ron Lowman, Strategic Marketing Manager, Synopsys
12:00 - 1:30	**Lunch**

	Physical Implementation	STA / ECO	Automotive	AMS Simulation	Prototyping / System
1:30 - 3:30	**Multiple Power Domain Design Planning Using IC Compiler II** MStar	**POCV: The Total OCV Solution from Synthesis, Implementation to Sign-off** MediaTek	**Automotive IP Design / Verification Flow** Synopsys	**SoC & IP System Verification Methodology with XA-VCS Cosim** Novatek	**Rapid Digital Signal Camera Prototyping System with Synopsys Auto-Partition Solution** iCatch
	ICCII Speed Up Physical Implementation of a High-Performance Design Amlogic	**Incremental Signoff Features in Physical-Aware Timing ECO Flow** MediaTek		**TSMC and Synopsys CustomSim Collaboration in New Measurement Approach for FinFET SRAM Design** TSMC	**Real-Time 4K 120Hz Video Display SoC Prototyping System Using HAPS-80 and ProtoCompiler** Himax
	TSMC/Synopsys Collaboration on 10nm Physical Implementation Enablement Paves the Path to 7nm TSMC	**How Do Easy ECO for DFFs' Default Values Change Without Dummy Cells?** PowerChip **Quick Timing Closure and Power Improvement with PrimeTime ECO** Synopsys	**Automotive Solution for ISO 26262** Synopsys	**AMS Verification Solutions: From CustomSim, VCS-AMS Simulation to Verdi-AMS Debugging** Synopsys	**Multi-FPGA Debug Strategy with Synopsys Physical Prototyping Platform – ProtoCompiler and HAPS-80 Systems** Synopsys
3:30 - 4:00	**Break**				

	Physical Implementation	Software Quality and Security	Verification	AMS Simulation	Prototyping / System
4:00 - 6:00	**Emerging Node Design with IC Compiler II / IC Validator, Accelerating Time-to-Market with Class Leading QoR** Synopsys	**Synopsys SIG Solutions for Software Quality and Security** Synopsys	**An Efficient Methodology to Achieve Accurate IR Analysis in Early Stage** Realtek	**Achieving High Library Quality for Design Robustness by SiliconSmart** Himax	**Adapt, Port, and Integrate Quickly – Prototyping the Right Way** Synopsys
	Managing Metal Fill and Its Impact on Your Design – Track Based Metal Fill with IC Compiler II and IC Validator In-Design Synopsys		**Key Techniques to Speed-up Debug and Verification Closure – Recent Innovations in Verdi** Synopsys	**Automatic Eye-Diagram Analysis and Jitter Measurement Using Custom WaveView ADV** Synopsys **Achieve High Quality Design with HSPICE, FineSim SPICE, Custom WaveView ADV for Signal Integrity, and Waveform Post-Processing** Synopsys **Simulation and Analysis Environment (SAE)** Synopsys	**Applying UPF 3.0 for Early, System-Level Power Analysis of SoCs with Micron DDR Memories** Synopsys
6:00 - 6:30	**Lucky Draw**				