# SNUG Singapore 2016 · Friday, August 19, 2016 · Parkroyal on Beach Road

## Don't Miss Out! SNUG Singapore Highlights and Special Events

- Attend the keynote by Dr. Chi-Foon Chan, President & co-CEO, Synopsys, Inc.
- Choose from over 25 technical presentations on advanced technologies and design styles by Users and Synopsys experts
- Network and connect with Synopsys executives and members of the local design community

| | Implementation Track I | Implementation Track II | Implementation Track III | Verification Track |
|---|---|---|---|---|
| **8:00 - 8:50** | **Registration** | | | |
| **8:50 - 9:55** | **Synopsys Keynote:** Dr. Chi-Foon Chan, President & co-CEO, Synopsys, Inc. | | | |
| **9:55 - 10:15** | **Tea Break** | | | |
| **10:15 - 10:45** | **Disruptive Techniques for Area Reduction in Hierarchical Chip**<br>MediaTek | **Automatic Feed-Through (FT) Compiler**<br>MediaTek | **Power Related ATE Fails During Transition Test: A Case Study** | **Advanced SoC Verification with Software Controlled Verification IP** |
| **10:45 - 11:30** | **Galaxy RTL: Design Compiler Family 2016.03 Update & Best Practices for Faster Runtime on Large Designs**<br>Synopsys | **IC Compiler II Delivers 10-20% Better Performance Power Area (PPA) on Advanced Designs**<br>Synopsys | **Address Testability Issues Early with SpyGlass DFT ADV**<br>Synopsys | **Essential Ingredients of Formal Verification**<br>Synopsys |
| **11:30 - 12:00** | **ICC VA Aware Port Punching** | **PFET Enabling Hook Up Scheme to Balance Between Peak Rampup Current, Rampup Time and PFET Transient FiSH Temperature** | **Grid-Based Scan Enable Logics Replication for High Speed Scan Launch-on-Shift Convergence** | **Complementing UVM Simulation with Formal Verification to Reduce Verification Cycle and Increase Verification Quality** |
| **12:00 - 13:00** | **Lunch** | | | |
| **13:00 - 14:00** | **Vision Address:** Mr. Don Chan, Vice President, Corporate Applications Engineering, Design Group, Synopsys Inc. | | | |
| **14:00 - 14:45** | **Emerging Node Design with IC Compiler II / IC Validator**<br>Synopsys | | **Static Analysis with SpyGlass**<br>Synopsys | **Achieving Higher Performance and Productivity with Native Integration of Simulation Flows**<br>Synopsys |
| **14:45 - 15:00** | **Tea Break** | | | |
| **15:00 - 15:30** | **Placement Guide Methodology for Better Placement Performance in ICC**<br>Realtek | **SoC Physical Implementation Challenges Using Mixed ICC2 and ICC1**<br>MediaTek | **Breaking into the FDSOI Realm: Design Methodologies that Help Designers Succeed in GLOBALFOUNDRIES 22FDx Technology**<br>GLOBALFOUNDRIES | **Is Gate Level Simulation Still Relevant in Verification Cycle?** |
| **15:30 - 16:00** | **20nm Custom Digital Circuit Structured Layout Auto Route with IC Compiler** | **Virtual Partition Flow for Rapid Design Convergence** | **At-Speed, All-Around Hierarchical Signoff with PrimeTime Hyperscale**<br>MediaTek | **System-Level Performance Verification of Multi-Core SoC** |
| **16:00 - 16:45** | **Custom Design Technology/Simulation Analysis Environment**<br>Synopsys | **Floorplanning Large Blocks Using IC Compiler II**<br>Synopsys | **PrimeTime ECO Tutorial**<br>Synopsys | **Key Techniques to Speed-Up Debug and Verification Closure – Recent Innovations in Verdi**<br>Synopsys |
| **16:45 - 17:15** | **Best Paper Awards & Lucky Draw** | | | |