SNUG India 2016 · July 13 – 14 · Leela Palace, Bangalore

Don't Miss Out! SNUG India Highlights and Special Events

- Attend the opening Keynote by Deirdre Hanford, Executive Vice President, Customer Engagement, Synopsys
- Choose from over 55 technical presentations on advanced technologies and design styles by Users and Synopsys experts
- Network and connect with Synopsys executives and more than 3000 members of the local design community

DAY 1 - July 13th 2016

7:30 - 8:45	**Registration and Breakfast**			
9:00 - 10:15	**Welcome:** Arindam Ghosh, Director, Applications Consulting, Synopsys **Keynote Address: "Innovation in the Age of Smart Everything"** – Deirdre Hanford, Executive Vice President, Customer Engagement, Synopsys			
10:15 - 10:30	**Break**			
	IC Verification	**IC Implementation**	**IC Design: Signoff**	**IC Design: FPGA & Test**
10:30 - 12:30	**Essential Ingredients of Formal Based Verification Signoff** Synopsys	**Floorplanning Large Blocks Using IC Compiler II** Synopsys	**PrimeTime ECO Tutorial** Synopsys	**Novel Approach for Power Island Emulation in FPGA Platforms** **How ProtoCompiler Helps Us in Addressing Some of Our Prototyping Challenges** NVIDIA
	Formal Datapath Verification Against SLM	**Leveraging Multi-Level Physical Hierarchy Ability for Quick & Predictable Concurrent Pin Placement in a Hierarchical Design Using Next Generation Physical Design Planning Tool**	**Evaluation of HyperScale & Physically Aware ECO Flows on Multi-Million Hierarchical Design**	**Accelerate Your Prototyping Productivity Leveraging HAPS with ProtoCompiler** Synopsys
	Validation of Dynamic Clock Gating Designs Using Hierarchical Sequential Equivalence Checking Qualcomm, Synopsys	**Advanced Low Power, Multi-Million Design Planning Using IC Compiler II** MediaTek, Synopsys	**SSD SoC – Low Power Multi-Voltage Timing Closure Challenges** Broadcom, Synopsys	
12:30 - 1:30	**Networking Lunch**			
1:30 - 3:15	**Automated Code Coverage Waiver File Generation – Speed Up Verification Signoff** NVIDIA, Synopsys	**Advanced Synopsys UPF-Based Flow to Perform Implementation & Verification** Synopsys	**PrimeTime Based Optimal Power Optimization Methodology for FinFET-Based Designs** AMD	**Advancement in ATPG Technology & Case Studies** Synopsys, Toshiba, STMicroelectronics, Broadcom, SGS-TUV
	System Level Coherency Verification for Configurable Coherent Interconnects Broadcom, Synopsys	**Low Power Implementation Challenges in a Highly-Power Critical SoC** Broadcom, Synopsys	**An Effective Debugging of Clocks Issues for Faster Design Closure** STMicroelectronics	
	Reuse of SystemC Models in RTL Verification NVIDIA	**Evolved Supply Set Based UPF Methodology** Seagate, Synopsys	**What's New in StarRC: Advances for Improving Productivity and Efficiency** Synopsys	
3:15 - 3:30	**Break**			
3:30 - 5:15	**Improving SoC/IP Quality Through RTL Design Parameter Analysis & Verification** NXP, Synopsys	**Design Compiler Family 2016.03 Update & Best Practices for Faster Runtime on Large Designs** Synopsys, Qualcomm, AMD	**Automation in Timing Exception Generation & Validation** AMD	**DFT Implementation Techniques for Multi-Power Domain Designs** Seagate
	ABV with Bugscope – Quicker, Easier, Worthwhile! NXP		**Advanced Reporting with PrimeTime** Synopsys	**Early RTL Testability & ATPG Coverage Analysis Using SpyGlass: A Case Study** Texas Instruments
		A Comprehensive CTS & Physical Aware Multibit Register Synthesis Methodology Qualcomm		**A Case Study on Launch – Off Extra Shift Implementation on DFTMAX Ultra Base Design** Broadcom
5:15 - 8:15	**Networking, Cocktails & Dinner with Entertainment by PunchTantraa (5:30 pm – 8:15 pm)**	**PrimeTime SIG (5:30 pm – 8:15 pm)**	**Networking, Cocktails & Dinner with Entertainment by PunchTantraa (5:30 pm – 8:15 pm)**	**Networking, Cocktails & Dinner with Entertainment by PunchTantraa (5:30 pm – 8:15 pm)**

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DAY 2 - July 14th 2016

	IC Implementation	IC Verification	AMS	Systems & IP / Academia
7:30 - 8:45	**Registration and Breakfast**			
9:00 - 10:15	**Welcome:** Girish Nanappa, Sales Manager, Synopsys **Keynote Address: "The Art of All Programmable Computing"** – Vamsi Boppana, Vice President, Processing, Systems, Software and Applications, Site Director and CTO, Xilinx India			
10:15 - 10:30	**Break**			
10:30 - 12:30	**From Nanometers to Ångstroms, Physical Design in the Next Decade** Synopsys	**Key Techniques to Speed Up Debug and Verification Closure – Recent Innovations in Verdi** Synopsys	**Custom Compiler – Under the Hood R&D Walk-Through** Synopsys, STMicroelectronics	**Transition to SystemC: Challenges and Benefits** NVIDIA
				Verification of Automotive Complex Generic Timer Module (GTM-IP) at Pre-Silicon Phase Bosch Engineering and Business Solutions
	Enhancing PPAS on High-Performance GPU Core with Next Generation PNR Tool	**Using Verdi HW SW Debug to Accelerate SW Development** Analog Devices, Synopsys	**Comprehensive IP Circuit Reliability Using CustomSim Monte-Carlo & MOSRA** STMicroelectronics	**Migrating to Synopsys ARC EM Processor for Accelerating Automotive Safety Product Designs** Analog Devices
	Holistic Approach from Place to Post Route Optimization Targeting High Performance Design Closure Using IC Compiler II in New SI Technologies Qualcomm, Synopsys	**System Firmware Validation (SFV) – A Certitude Approach** Qualcomm	**Challenges & Practical Lessons Learnt from Mixed Signal Verification of Multi-Protocol Compliant DDR PHY in 14nm LPP Process Node** Rambus Chip Technologies, Synopsys	**Optimizing User Software Using ARC Processor Extensions (APEX) in ARC EM Processors** Synopsys
12:30 - 1:30	**Networking Lunch**			
1:30 - 3:30	**IC Compiler II 2016.03 Technologies to Meet Aggressive Performance, Power & Area Goals** Synopsys	**Recent Advancements in SpyGlass CDC & RDC** Synopsys	**Advanced Characterization Features in SiliconSmart** Synopsys	**SHAKTI – A Microprocessor Development Initiative** IIT Madras
	A Comprehensive Strategy to Resolve Design & Methodology Issues in High Performance ASICs Broadcom	**Robust RDC Verification & Architectural Solutions to Eliminate Metastability Issues** NXP	**Implementing a SiliconSmart Based Flow for Characterizing DDR PHY Blocks** Qualcomm	**Multi-Scale Modeling of $Si_{1-x}Ge_x$ FinFETs: A Case Study of Material-to-Device Modeling** IIT Bombay
	Experience of Delivering Improved PPA & Closure Time Using IC Compiler II in High Performance x86-Microprocessor Design AMD	**Augmenting Test Logic Validation Using Static Connectivity Verification** STMicroelectronics, Synopsys	**A Novel Approach to Reusable & Time Economized Methodology for Analysing DDR3 & DDR4 SSO Measurement Using Custom WaveView ADV** Microsemi, Synopsys	
3:30 - 3:45	**Break**			
3:45 - 5:15	**Developing the Next Generation P&R Flow for Complex Networking Designs**	**An Efficient Hierarchical Abstract Flow Approach for SoC Netlist Design** Broadcom	**NanoTime for Multi-Cycle Multi-Throughput Large Memory with Complex Design Challenges** NVIDIA	**Formal Methods in EDA: Looking Beyond the Traditional Bastions** IIT Kharagpur
	Strategies to Implement Clock Tree Synthesis for Multiple Power Domain Design Seagate		**Augmentation of Static & Dynamic Checks for Electrical Verification of Mixed Signal Circuits** AMD	**Ultra Low Voltage Design: Challenges and Opportunities** IISc
5:15 - 5:45	**Best Paper Awards & Lucky Draw**			