SNUG Germany 2016 · Thursday, June 23, 2016 · Hilton Munich City

Don't Miss Out! SNUG Germany Highlights and Special Events

- Over 35 technical presentations on advanced technologies and design styles by Users and Synopsys experts
- Keynote by Ravi Tembhekar, Vice President, Corporate Application Engineering, Design Group, Synopsys, Inc.
- Opportunities to connect with Synopsys executives and members of the local design community

8:00 - 9:00	**Registration and Breakfast**					
9:00 - 10:15	**Welcome and Introduction:** Frank Poppen, OFFIS Institute for Information Technology & SNUG Europe Technical Chair **Synopsys Keynote:** Ravi Tembhekar, Vice President Corporate Application Engineering, Design Group, Synopsys, Inc.					
10:15 - 10:45	**Break**					
	Digital - Implementation	**Digital - Test & Signoff**	**Digital - Verification**	**Custom & AMS**	**System & Analog Verification**	**Demo**
10:45 - 12:15	**Entering FD-SOI Era - Ease of Design Combined with Tunable Performance/Power Optimization Using GLOBALFOUNDRIES 22FDx Technology** GLOBALFOUNDRIES	**Optimisation of DFTMAX Ultra Scan Patterns** Dialog Semiconductor	**One SoC, Two Verification Methods (Formal and Simulation), One Common Coverage Metric** NXP Semiconductor	**Development and Verification of a Truly Interoperable PDK at ams** ams AG	**Automated Integration of MathWorks® Simulink® Signal Flow Graph Models into Synopsys® VirtualizerTM-based Virtual Prototypes** Robert Bosch GmbH, The MathWorks GmbH, The MathWorks, Inc.	**Mixed-Signal Simulation Debug Automation using Verdi** Synopsys
	Reduce Chip Area in a High Routing Congested ARM CortexM3 Design Micronas New Technologies	**Increasing Test Coverage with Dedicated Scan Enable for ICG's** Dialog Semiconductor, Synopsys GmbH	**Enriching Your Simulation Work Flow with Behavioral SystemC Models** DMCE GmbH & Co KG	**Standardized PDK Setup in Design Projects** Micronas GmbH	**Deploying the ProtoCompiler Tool for Targeting Complex FPGA-based Prototyping Platforms in a Highly Automated Approach** JSC Baikal Electronics, Synopsys GmbH	**Q&A**
	Gated Power Network Design and Implementation of High-End ARM® GPU Cores in Mission and Scan Modes JSC Baikal Electronics, Synopsys	**How Logic and Memory BIST Can Help to Address Some Functional Safety Requirements in Automotive ICs** Robert Bosch SAS	**The S32V234 Vision Processor VDK: A Virtual Prototype for ADAS Applications** NXP Semiconductor, Synopsys	**De-Mystifying TCL Custom Application Creation in Custom Compiler, with Automatic AMS IP Block Documentation as an Example** Elmos Semiconductor AG	**FPGA Prototyping of a Complete System-on-Chip with the HAPS-DX7** Hyperstone GmbH	**RTL & Embedded Software Debug with Verdi HW/SW** Synopsys
12:15 - 13:30	**Lunch**					
13:30 - 15:00	**Partial State Retention with Scan Chains** Toshiba Electronics Europe GmbH	**Bottom-up Reusable Timing Constraints Development and Validation Methodology in Case of Multiplexed External Interfaces** Axis Communications AB	**Yet Another Memory Manager (YAMM)** AMIQ Consulting SRL	**A SPICE based MOSFET Calculator** Micronas GmbH	**CCK GUI Integration Flow – Custom Voltage Domain Checks to Catch Real-Life Tapeout Killers** Dialog Semiconductor	**Using a HAPS-80 Platform for Traffic Sign Recognition Application (+ Verdi Debugging)** Synopsys
	Generating Accurate Gate Level Activity for Power Analysis, Prior to Back Annotated Timing Simulation Infineon Technologies AG	**Logical and Physical Isolation using UPF Including DFT Requirements** IDT	**Mastering Reactive Slaves in UVM** Verilab	**SAE Based Top Level Verification of CMOS Analog Circuits** Micronas GmbH	**Innovative Propagation Methodology for Diodes and Clamps by Using TCL-CCK Advanced Capabilities in Synopsys Circuit Check** STMicroelectronics, Synopsys	**Q&A**
	Quo Vadis Power? Early Power Assessment over Development Cycle Infineon Technologies AG	**PCI Express DesignWare Ctrl IP Core Power Estimation and Profiling with SpyGlass** Synopsys	**Essential Ingredients of Formal Based Verification Signoff** Synopsys Professional Services	**Incorporating System Verilog Real Number Models in Mixed Signal Simulation (VCS AMS) with Advanced Analog Mixed Signal Debug (Verdi AMS) and Utilizing Re-usable System Verilog Testbenches** Synopsys	**System Level Verification with CustomSim PCM (Phase Change Memory) Built-in Cell** STMicroelectronics, Synopsys	**Using a HAPS-80 Platform for Traffic Sign Recognition Application (+ Verdi Debugging)** Synopsys
15:00 -15:30	**Break**					
15:30 - 17:00	**Floorplanning Blocks Using IC Compiler II** Synopsys		**Static Analysis with SpyGlass** Synopsys	**Custom Compiler – Latest Innovations in Custom Design for Advanced Nodes Walk-Through** Synopsys	**An Introduction: Programmable Extended Electrical Rule Checking in IC Validator** Synopsys	
	ICC II GUI Tutorial: New Technology in ICCII IDE Simplifies Design and Boosts User Productivity Synopsys			**Custom Compiler - Walkthrough of SAE: The New Simulation Analysis Environment in the Latest Release of Hspice, Finesim and CustomSim** Synopsys	**Extended ERC for Full Chip Verification to Avoid ESD and Design Related Pitfalls** ELMOS Semiconductor AG	
17:00 -18:30	**Awards & Refreshments**					