SNUG Austin 2016 · Thursday, September 29, 2016 · Hilton Austin

8:00 – 8:45	**Registration and Breakfast**					
8:45 – 10:15	**Welcome and Introduction:** Jeff Montesano, SNUG Austin Tech Chair – Verilab **Synopsys Keynote:** "Innovation in the Age of Smart Everything" – Deirdre Hanford, Executive Vice President, Customer Engagement – Synopsys					
10:15 – 10:30	**Break**					
	Frontend Implementation	**Backend Implementation**	**Digital Verification I**	**Digital Verification II**	**FPGA/Prototyping**	**Test**
10:30 – 12:30	**Improving Timing and Power with PrimeTime ECO Flows** Synopsys	**Best Practices for High-Performance, Energy-Efficient Implementations of the ARM® Cortex®-A73 Processor in 16-nm FinFET Plus (16FF+) Process Technology Using Synopsys Galaxy Design Platform** ARM, Synopsys	**Applying Stimulus and Sampling Outputs - UVM Verification Testing Techniques** Sunburst Design	**SystemVerilog: Reusable Class Features and Safe Initialization of Static Variables** Advanced Micro Devices	**Latch-Based CPU Prototyping with HAPS Platform**	**Synopsys Automotive Test Solution: Moving the DFT Needle Forward** Synopsys
	Black-Boxing Techniques for Improving VC-LP Throughput Advanced Micro Devices	**Floorplanning Large Blocks Using IC Compiler II** Synopsys	**Complex Constraints: Unleashing the Power of the VCS SystemVerilog Constraint Solver** Samsung	**Advanced X-Prop Usage for the NXP LS1080 Verification** NXP Semiconductors, Synopsys	**High-Level Performance Estimation on Virtual Prototypes Employing Timing Annotation** ARM	
			Configuring a Date with a Model - A Guide to Configuration Objects and Register Models Verilab	**Tough Bugs vs. Smart Tools - L2/L3 Cache Verification Using System Verilog, UVM, and Verdi Transaction Debugging** Centaur Technology, Synopsys	**Accelerate Your Prototyping Productivity Leveraging HAPS Integrated Prototyping Solution** Synopsys	
12:30 – 1:30	**Lunch**					
	Frontend Implementation	**Backend Implementation**	**Digital Verification I**	**Digital Verification II**	**Full Custom Implementation**	**Test**
1:30 – 3:00	**Design Compiler Update and Runtime Best Practices** Synopsys	**Best Practices for a Performance- and Area-Focused Implementation of High-Performance GPUs Using Galaxy Design Platform** Synopsys	**Unique Methodology to Streamline the Checking of Design Tie-Offs** NXP Semiconductors, Synopsys	**Molding Functional Coverage and Reporting for Highly Configurable IP** Broadcom	**Statistical Characterization Methodology to Design and Margin for 16nm FinFET Flops** NXP Semiconductors	**DFTMAX Ultra User Experience for Small, Digital, Mixed-Signal Devices** Maxim Integrated
	Effective Reporting and Analysis of Timing Results with PrimeTime Synopsys	**Updates and Best Practices for IC Compiler II with In-Design IC Validator** Synopsys	**Essential Ingredients of Formal Based Verification** Synopsys	**Effective SystemVerilog Functional Coverage: Design and Coding Recommendations** Verilab	**Power-Intent Verification Methodology in Multi-Voltage Domain Custom Memory Macro to Prevent Circuit Failures** Advanced Micro Devices, Synopsys	**DFTMAX Ultra: Achieve Additional Cost Reduction with Hardware-Assisted Shift Power Reduction** Synopsys
						Low-Power DFT and Effective Test Pattern Count Reduction in a Custom High-Performance Applications Processor Design Samsung, Synopsys
3:00 – 3:15	**Break**					
3:15 – 5:15	**ECO User Case Studies Using Formality Ultra** Synopsys	**Achieving Correlation Between Synthesis and Routed Design for High-Performance Block** Advanced Micro Devices	**Verifying Microprocessor Debug-Bus Connectivity Formally Using VC Formal** Advanced Micro Devices	**Leveraging LevelDB for Unit-Level Replay of Top-Level Stimulus in UVM** Samsung	**Custom Compiler Technology Walkthrough** Synopsys	**TetraMAX II: Reduce Test Cost by 25 Percent with 10X Faster Runtime** Synopsys
		Structural MSCTS Implementation Best Practices Advanced Micro Devices	**Using Formal Tools to Verify Datapath Designs During Various Phases of a Processor Development** Advanced Micro Devices, Oski Technology	**Layered Testbench Architecture for Serial Protocol Using UVM** einfochips, Synopsys		**TetraMAX II ATPG, Broadcom's Results and Experience** Synopsys, Broadcom
	Static Analysis with SpyGlass Synopsys	**Implementing a 150M+ instance Networking chip @28nm with Galaxy Platform** Synopsys	**The Lights in the Tunnel: Coverage Analysis for Formal Verification** Oracle, Synopsys	**Advanced Verification Techniques for the NXP LS1080 Memory Validation** NXP Semiconductors, Synopsys	**Walk-Through of SAE: The New Simulation Analysis Environment in the Latest Release of HSPICE, FineSim, and CustomSim** Synopsys	**Connectivity Validation with SpyGlass** Synopsys
5:15 – 6:30	**Awards and Evening Event**					