Radiation Hardened Electronics Technology (RHET)

Oct 25th, 2007 Clearwater, Florida

Designing Advanced ASIC’s with Synopsys Design Tool Suite

Synopsys Professional Services
Synopsys Inc.

Rick Hayden
Agenda

- Today’s Program Management challenges
- Today’s Technical design challenges
- Synopsys Tool Suites
- Synopsys Professional Services

HW& SW
Codevelopment

Reusable
Standard Hardware

Low Power
Consumption

Operating System
Drivers
Software applications

Digital
Hardware Design

Analog
Circuit Design
Today’s Program Management challenges
PM’s Role: Case Study

Sound familiar?
Uncertainty in Effort Estimates

- Early in the project you can have firm cost and schedule targets or a firm feature set, but not both.
- Cone of Uncertainty implies that it is not only difficult to estimate projects accurately in the early stages but theoretically impossible.
Managing Design Complexity

• Due to the nature of ASICs, nearly every design:
  ▪ Complete systems on a single die (SoC)
  ▪ Often requires 3rd party IP
  ▪ Mixed signal designs are becoming prevalent
    • SERDES, USB, PCIe, etc.
  ▪ Verification is more complex
  ▪ Requires leading edge silicon technology

• Accurate schedule and effort estimation is difficult to make in early stages of design:
  ▪ Design specification may not be solidified
  ▪ Unknowns in design flows, libraries, processes
  ▪ Integration of 3rd party IP can be underestimated
Today’s Technical design challenges
• Interconnect delay, delay due to crosstalk, and delay due to IR drop are more dominant in smaller technologies.
• Post-layout analysis with parasitics is required for accurate modeling.
Leakage Power becomes more dominant at smaller technologies.

- Leakage power becomes more dominant at smaller technologies.
- Multi-Vth libraries are used to provide balance between performance and leakage.
Design for Manufacturability & Yield

In sub-micron Wire-to-Wire Cap Dominates ($C_W >> C_S$)

- **Signal Integrity:** problems in design that affect your timing
  - Crosstalk / Static Noise
  - Voltage (IR) drop

- **Reliability:** long term current damages your chip
  - Electromigration

- **Manufacturability:** charge effects results in reducing yield
  - Process Antenna Effect
Synopsys Tool Suite
Synopsys Design Platforms

Discovery™ Verification Platform

Galaxy™ Design Platform

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Verification Challenge Fueling Growth

“Validation is the biggest challenge going forward, limiting our ability to do more complex designs”

Intel

“Over 50% of our chip design resources are now committed to Verification”

Texas Instruments
Language Fragmentation

- Design Size
- Gap
- Property
- Testbench
- Assertion
- Coverage
- Mixed-HDL
- C++
<table>
<thead>
<tr>
<th>Property</th>
<th>Assertion</th>
<th>Coverage</th>
<th>Language</th>
<th>Verification (Simulation)</th>
<th>Design for Verification</th>
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<td>Gap</td>
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Benefits of SystemVerilog for Design

- Easy communication between System Architects, Design Engineers and Verification Engineers
- Enables higher level of abstraction
- Provides code compaction
- Has specific language constructs that reduce mismatches between simulation, synthesis and formal verification tools
- Better Description of Hardware Specific Procedures
- Enhanced Readability
Galaxy™ Design Platform
Predictable Synthesis
Topographical (Physically Aware) Technology

- No need for WLMs
- Correlates to post-layout results
- Reduces iterations
- Easily adaptable into existing design flows

Enables fastest TTR and Better Start Point for P&R
Next-Generation Place and Route Solution
IC Compiler

Netlist

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<thead>
<tr>
<th>TCL</th>
<th>GUI</th>
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</thead>
<tbody>
<tr>
<td>Physical DFT</td>
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Milkyway

GDSII

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Global Technical Solutions

Pilot provides a mature, modular environment and flow to help maximize repeatability, efficiency, and productivity.

Quality checks and reviews ensure successful execution of projects according to plans.

DesignSphere compute infrastructure helps ensure worldwide team execution.
Predictable Success

GUI for ease of flow setup

Enable consistent multi-site, multi-project IC development

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Solutions to Reduce Program Risk

**Program Risk**
- EDA Tool License Shortages
- Compute Resource Limitations
- Engineering Skills & Resources Shortages
- Procurement of Reliable IP

**Solutions**
- EDA Tool Access by Program
- Scalable Compute Platforms
- Scalable Design Services (ITAR Compliant Resources)
- Robust, Proven IP Portfolio
Design Collaboration Environment
Scalable Infrastructure

- Collaborative design infrastructure
  - Enables customer, Honeywell and Synopsys engineers to act as single design center
    - Use a common Pilot flow
    - On-demand availability of tool licenses
    - ITAR Compliant

- Scalable data center
  - Server farm with 100’s of CPU’s
  - LSF based job launching for parallel computing
  - Regular back-ups
  - Physically secured and monitored 24x7x365