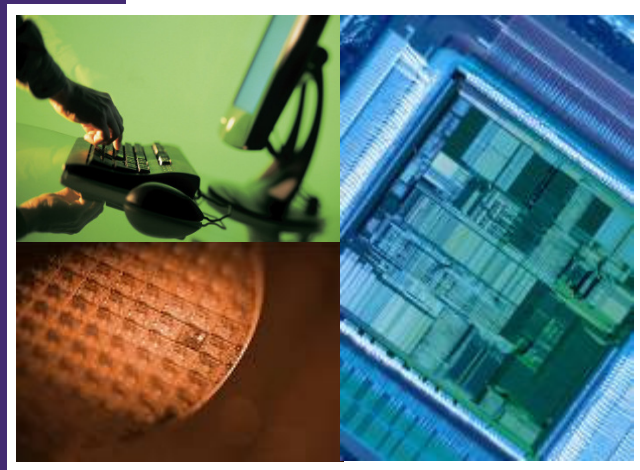
Radiation Hardened Electronics Technology (RHET)

Oct 25th, 2007 Clearwater, Florida

Designing Advanced ASIC's with Synopsys Design Tool Suite



Synopsys Professional Services
Synopsys Inc.

Rick Hayden

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Agenda

- Today's Program Management challenges
- Today's Technical design challenges
- Synopsys Tool Suites
- Synopsys Professional Services

HW& SW Co-development

Reusable Standard Hardware

Low Power Consumption

Operating System

Drivers
Software applications

Digital Hardware Design

Analog Circuit Design

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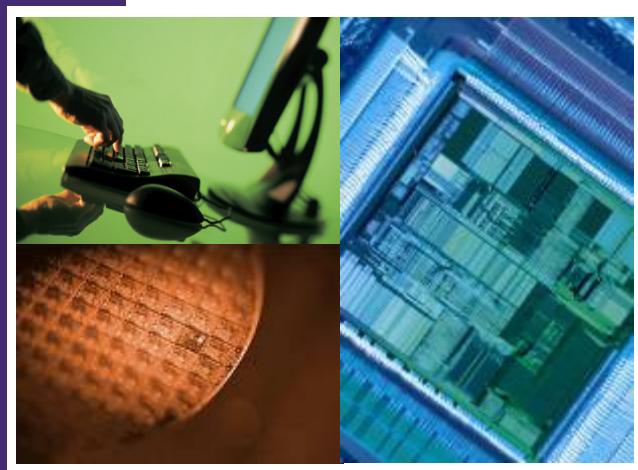
Today's Program Management challenges



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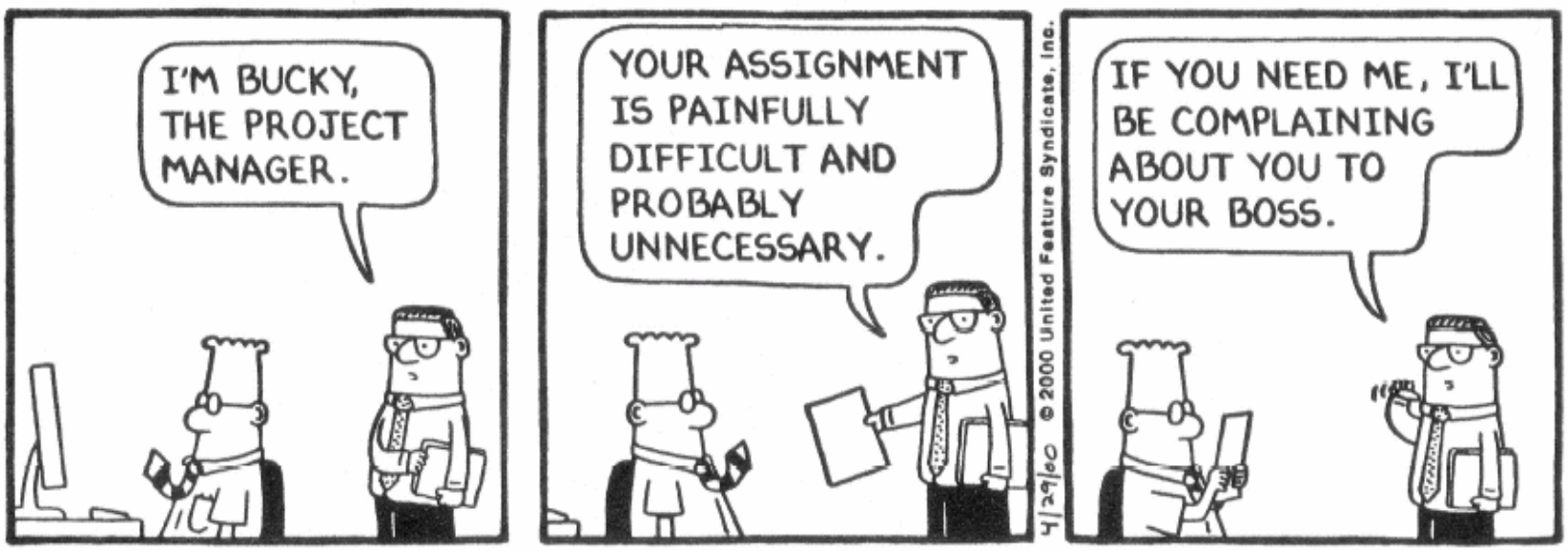
PM's Role: Case Study



Sound familiar?

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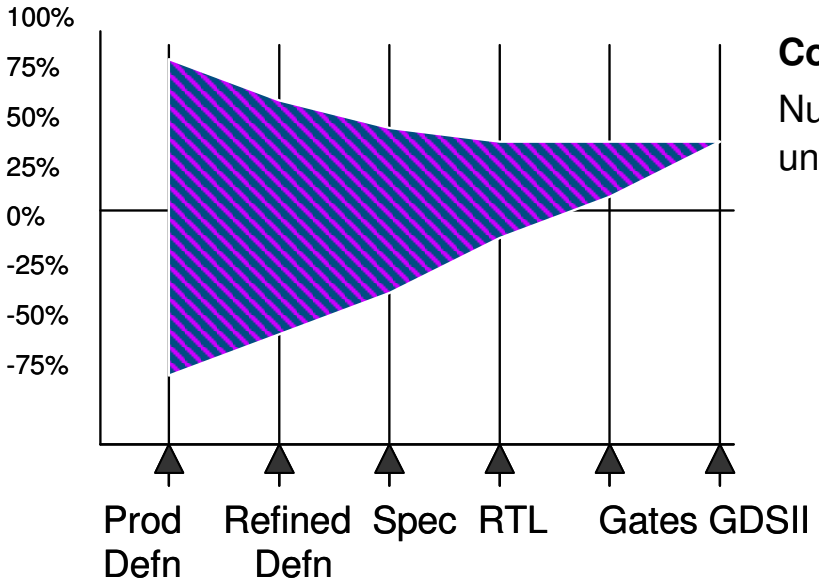
Uncertainty in Effort Estimates



Cone of Uncertainty

Number of unknowns and corresponding uncertainty in effort estimates through project life

- Early in the project you can have firm cost and schedule targets or a firm feature set, but not both.
- Cone of Uncertainty implies that it is not only difficult to estimate projects accurately in the early stages but theoretically impossible.

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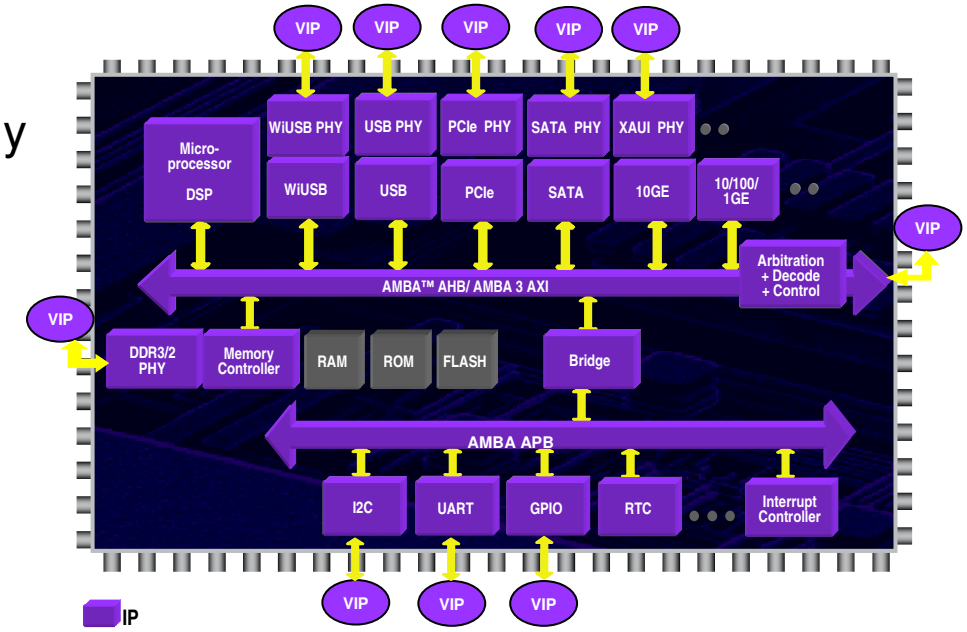
Managing Design Complexity

- Due to the nature of ASICs, nearly every design:
  - Complete systems on a single die (SoC)
  - Often requires 3rd party IP
  - Mixed signal designs are becoming prevalent
    - SERDES, USB, PCIe, etc.
  - Verification is more complex
  - Requires leading edge silicon technology

- Accurate schedule and effort estimation is difficult to make in early stages of design:
  - Design specification may not be solidified
  - Unknowns in design flows, libraries, processes
  - Integration of 3rd party IP can be underestimated



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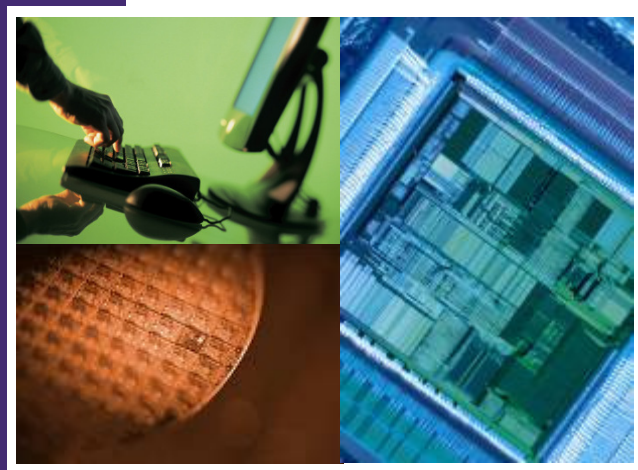
Today's Technical design challenges



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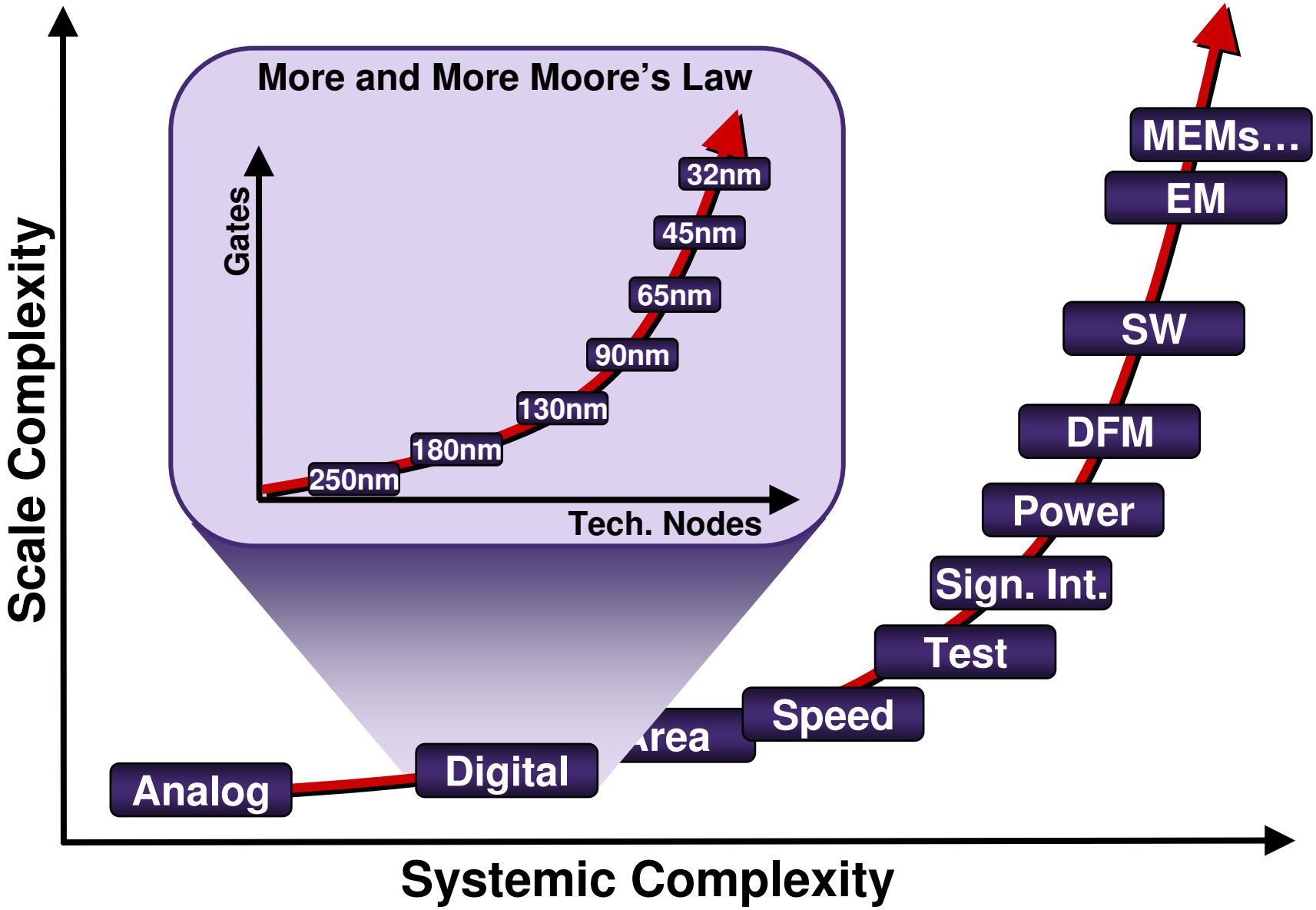

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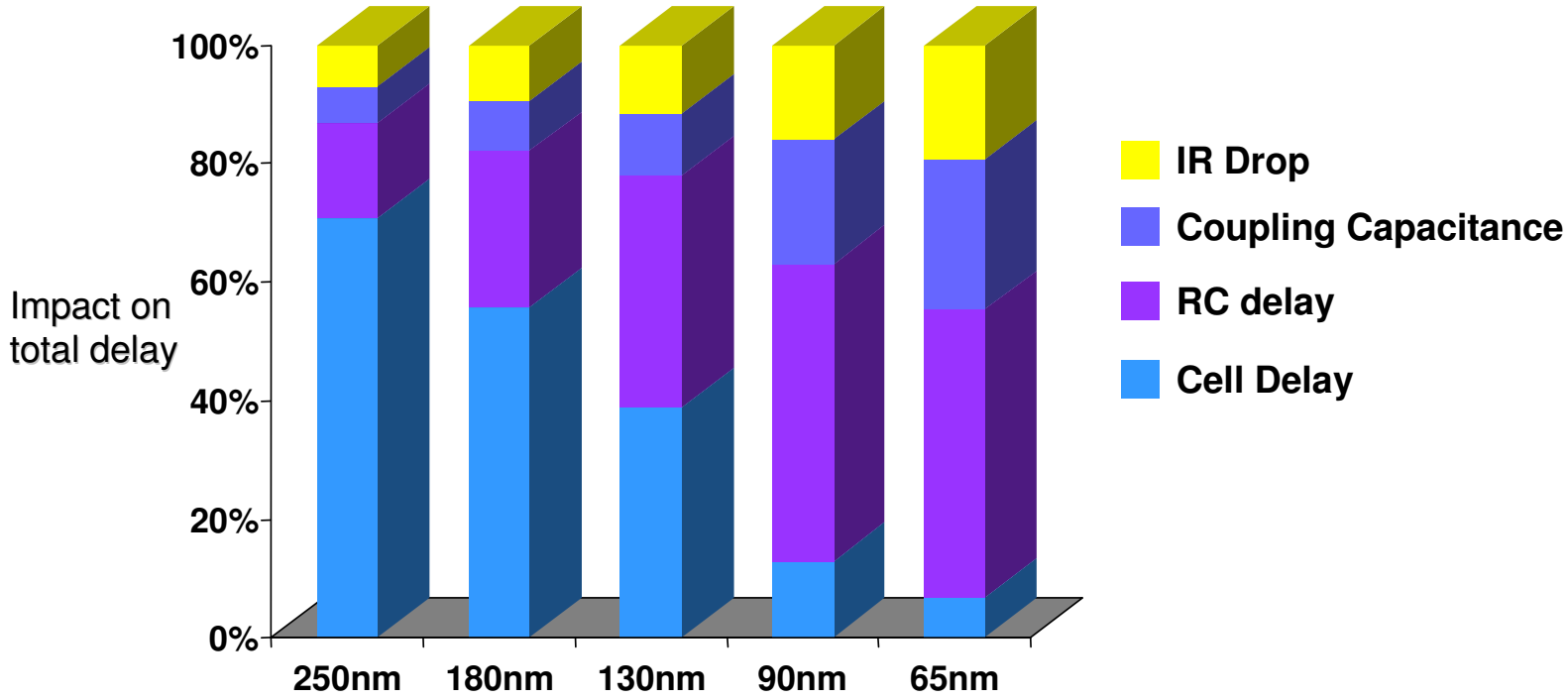
Design Performance Trends



- Interconnect delay, delay due to crosstalk, and delay due to IR drop are more dominant in smaller technologies.
- Post-layout analysis with parasitics is required for accurate modeling.

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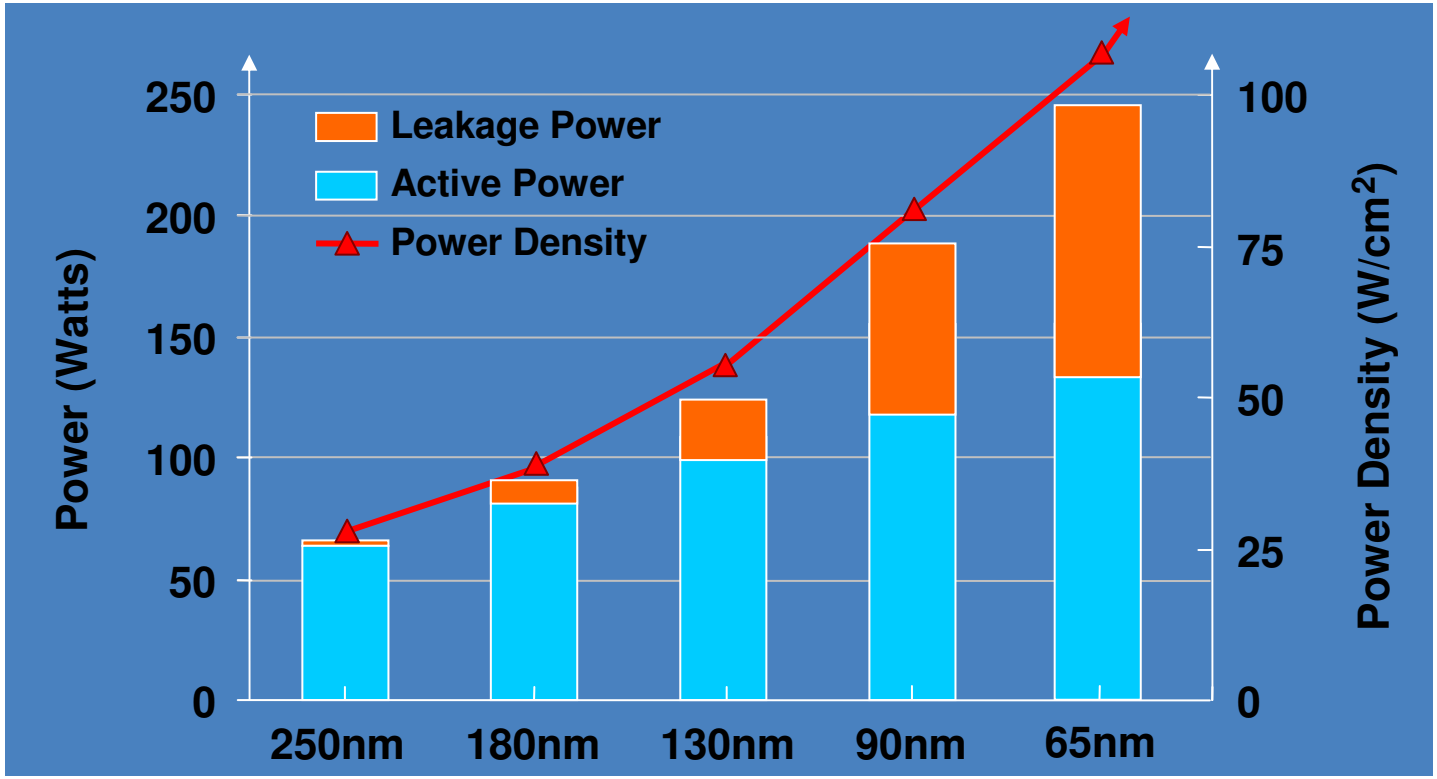
Leakage Power Trends



- Leakage power becomes more dominant at smaller technologies.
- Multi-Vth libraries are used to provide balance between performance and leakage.

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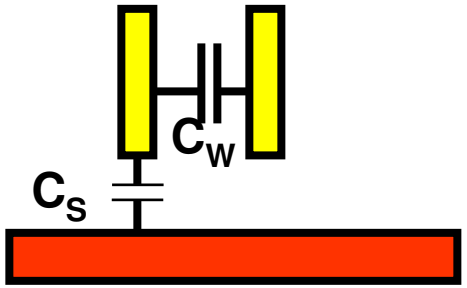
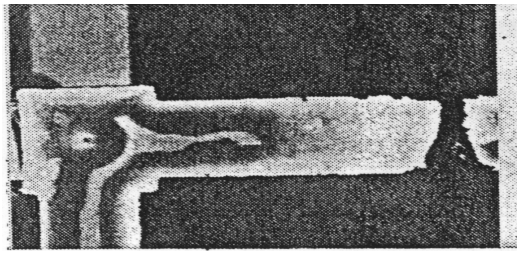
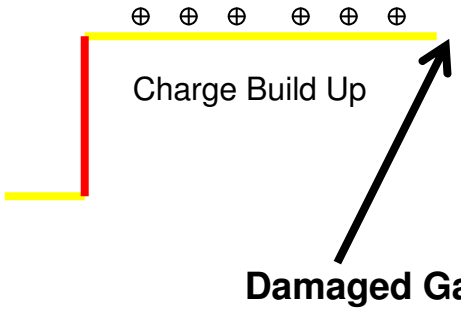
Design for Manufacturability & Yield

In sub-micron Wire-to-Wire Cap Dominates ($C_W >> C_S$)







- **Signal Integrity:** problems in design that affect your timing
  - Crosstalk / Static Noise
  - Voltage (IR) drop
- **Reliability:** long term current damages your chip
  - Electromigration
- **Manufacturability :** charge effects results in reducing yield
  - Process Antenna Effect

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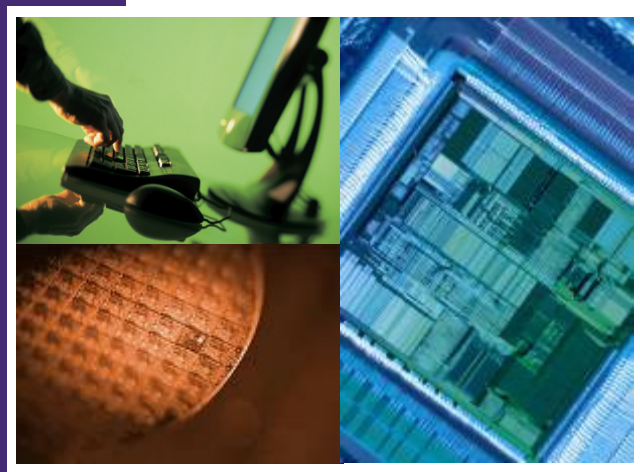
Synopsys Tool Suite



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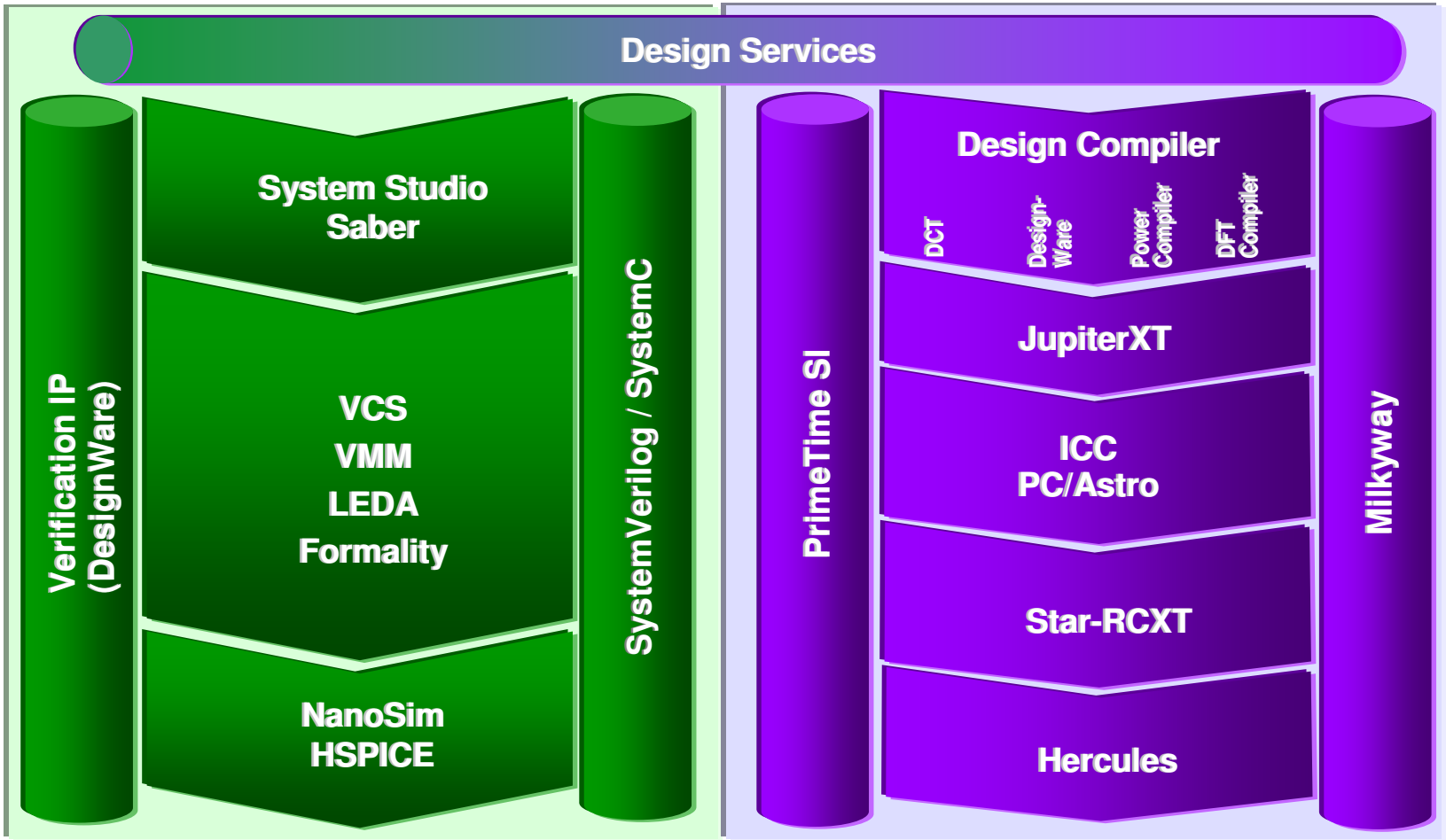
Synopsys Design Platforms



Discovery™ Verification Platform **Galaxy™ Design Platform**

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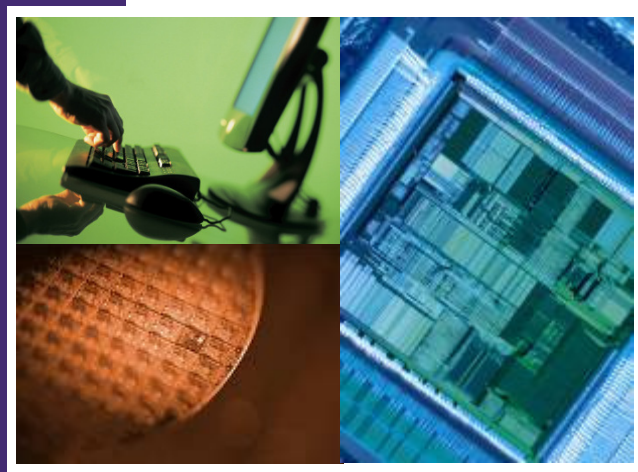
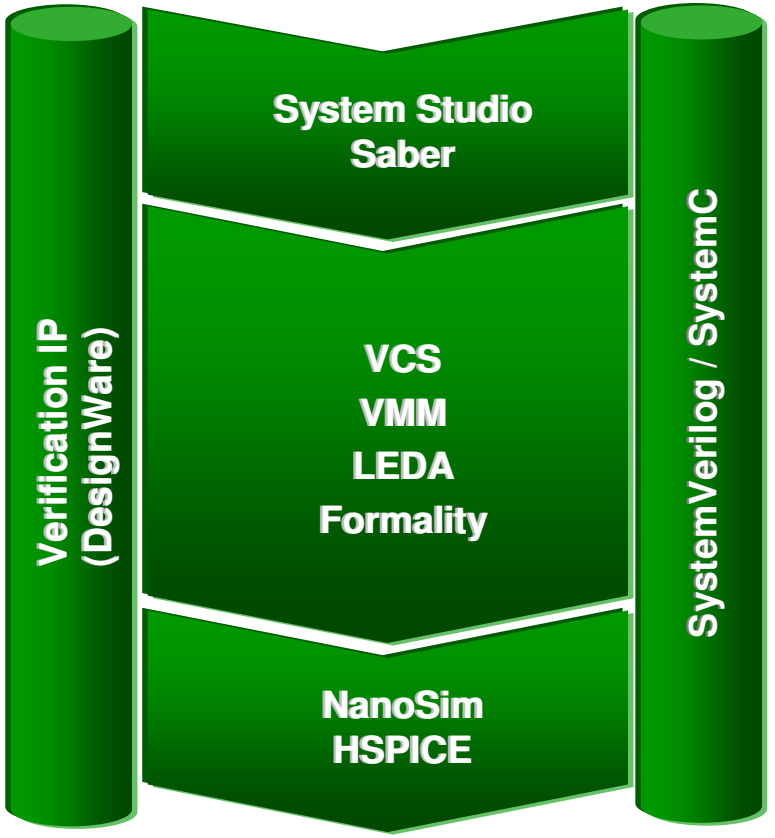
Discovery™ Verification Platform





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Verification Challenge Fueling Growth

"Validation is the biggest challenge going forward, limiting our ability to do more complex designs"

Intel

"Over 50% of our chip design resources are now committed to Verification"

Texas Instruments

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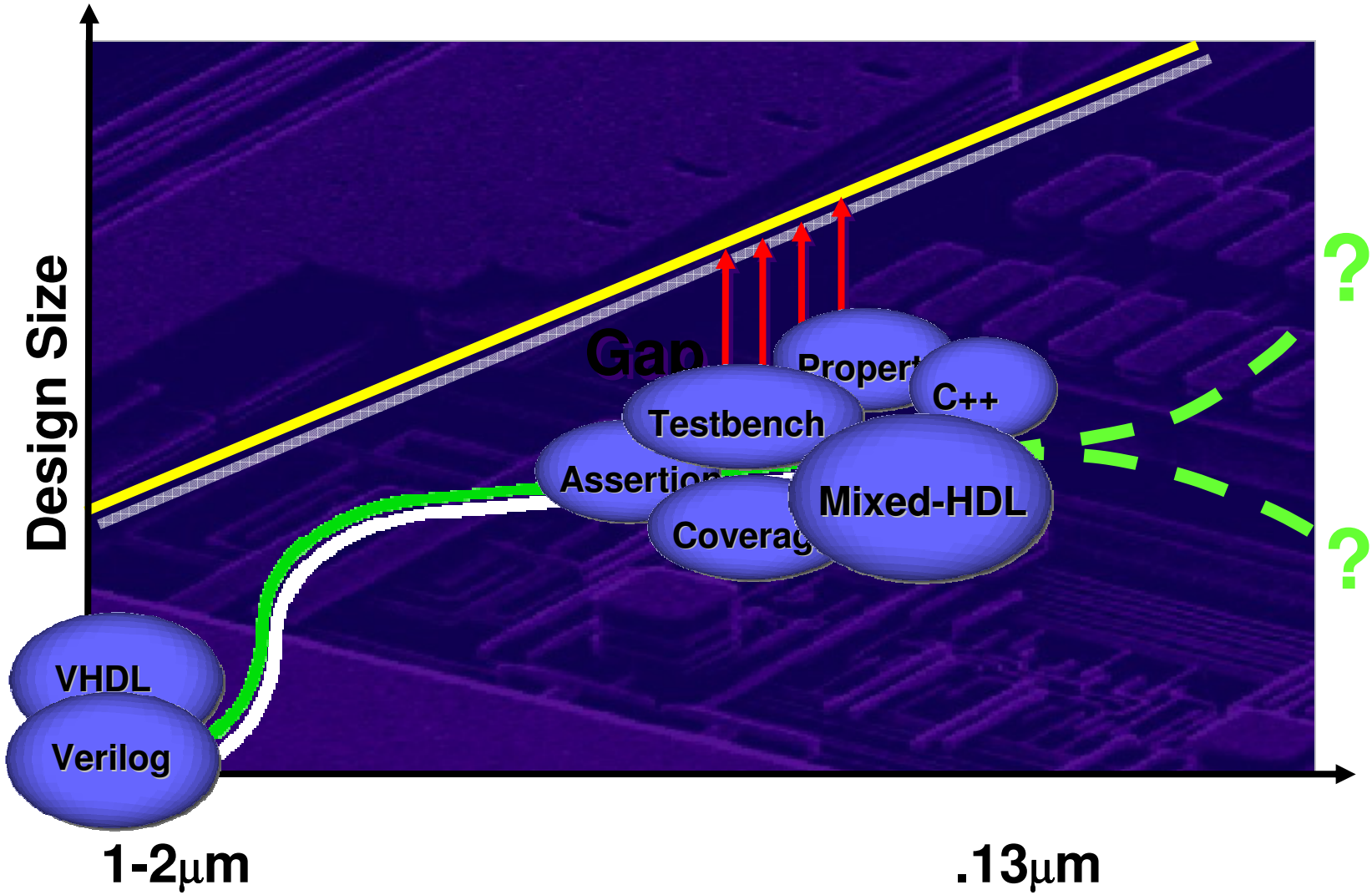
Language Fragmentation



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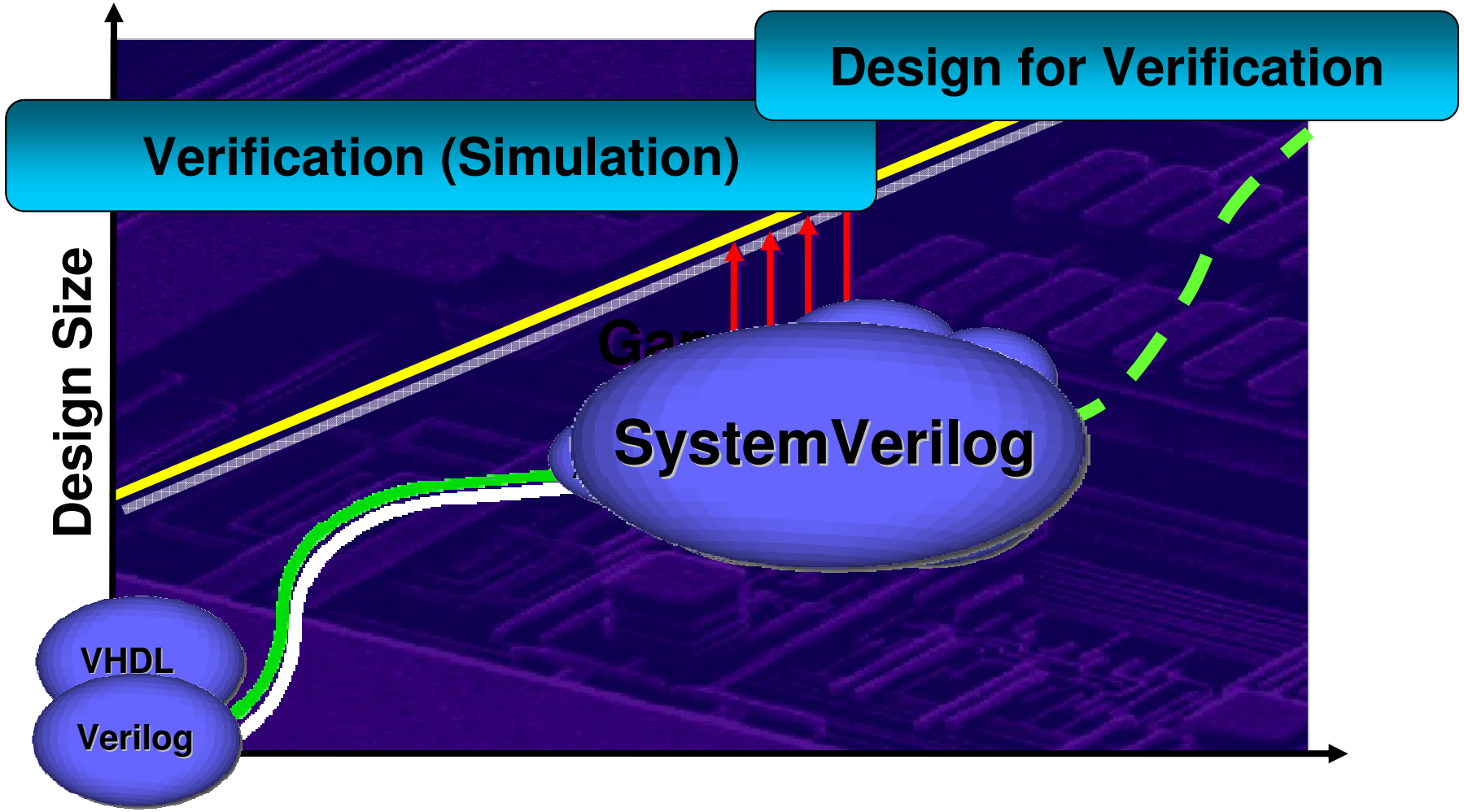
Standardization Opens DFV Age



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Benefits of SystemVerilog for Design

- Easy communication between System Architects, Design Engineers and Verification Engineers
- Enables higher level of abstraction
- Provides code compaction
- Has specific language constructs that reduce mismatches between simulation, synthesis and formal verification tools
- Better Description of Hardware Specific Procedures
- Enhanced Readability

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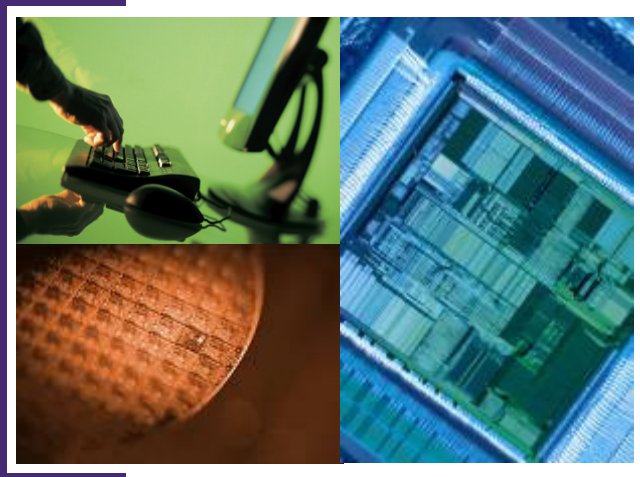
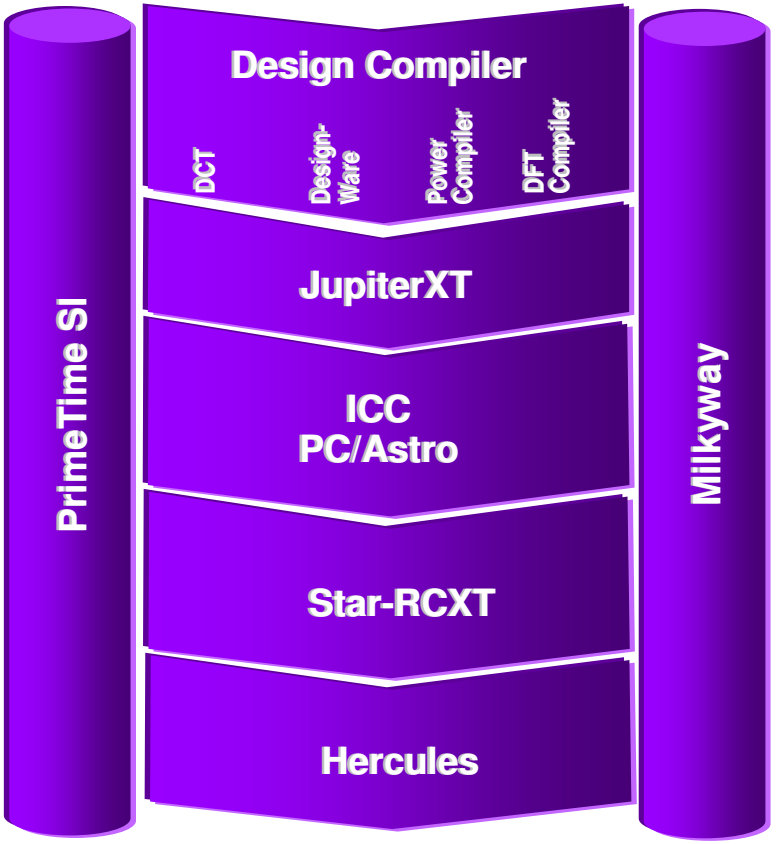
Galaxy™ Design Platform





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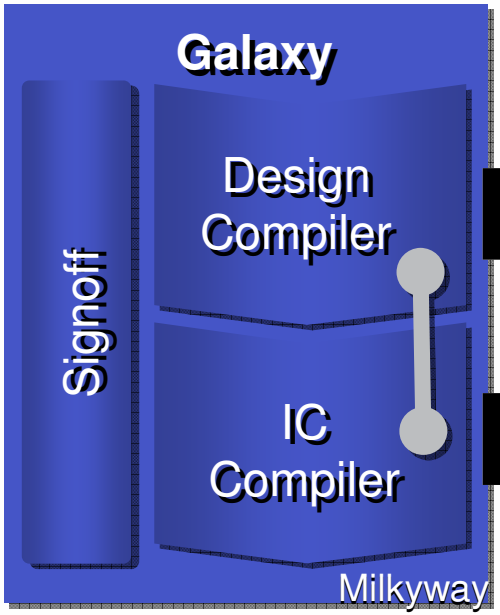
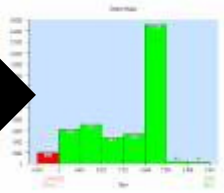
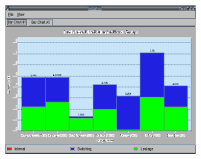
Predictable Synthesis
Topographical (Physically Aware) Technology

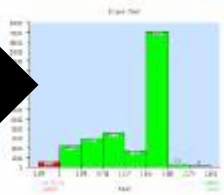


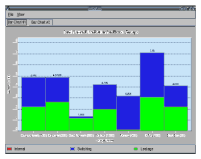
Timing & Area

Power









- No need for WLMs
- Correlates to post-layout results
- Reduces iterations
- Easily adaptable into existing design flows

Enables fastest TTR and Better Start Point for P&R

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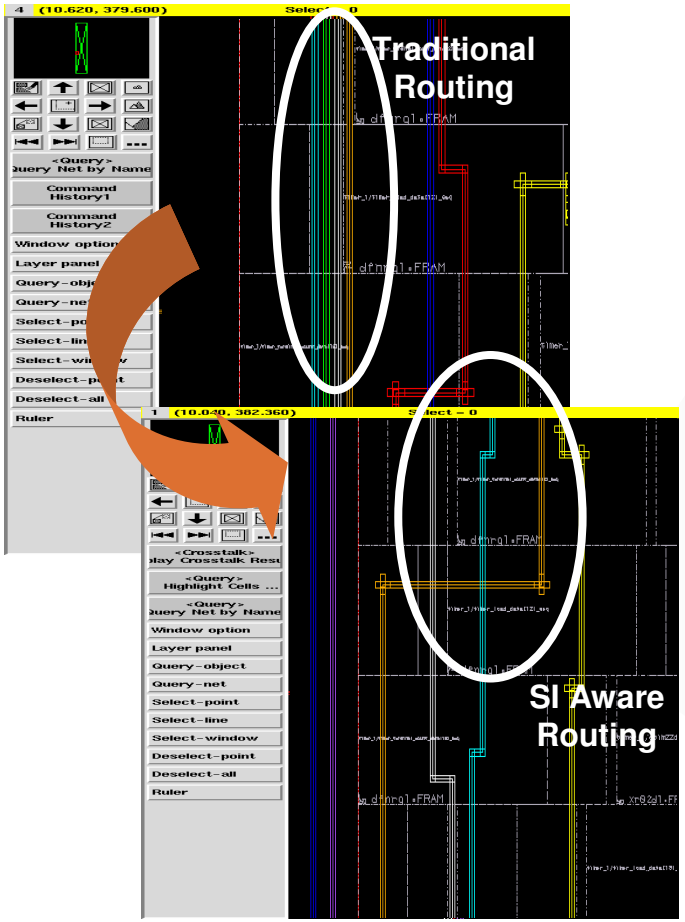
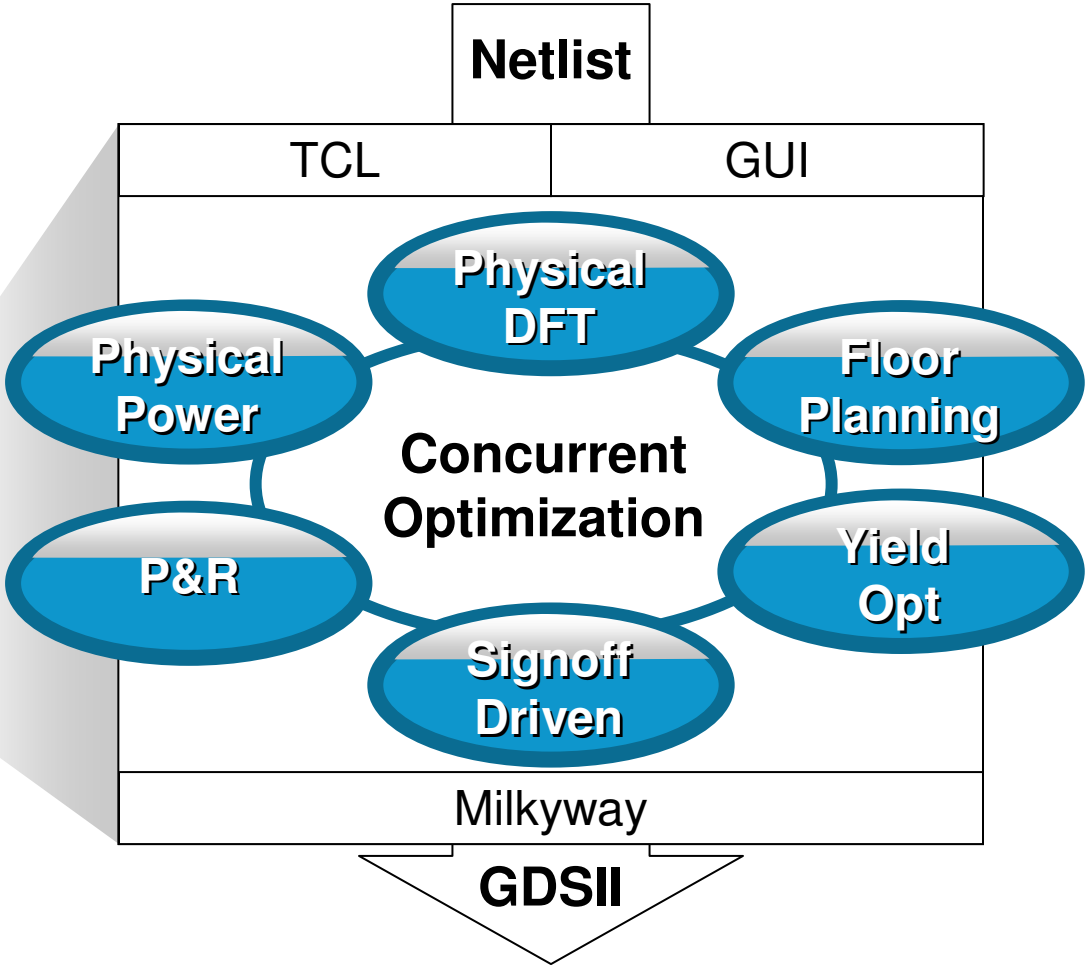
Next-Generation Place and Route Solution
IC Compiler





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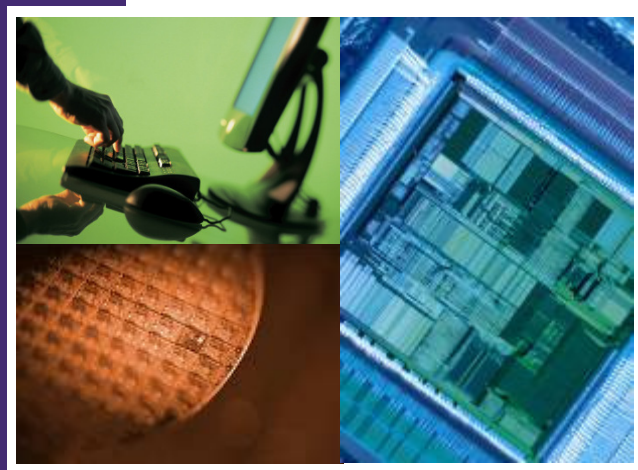
Synopsys Professional Services



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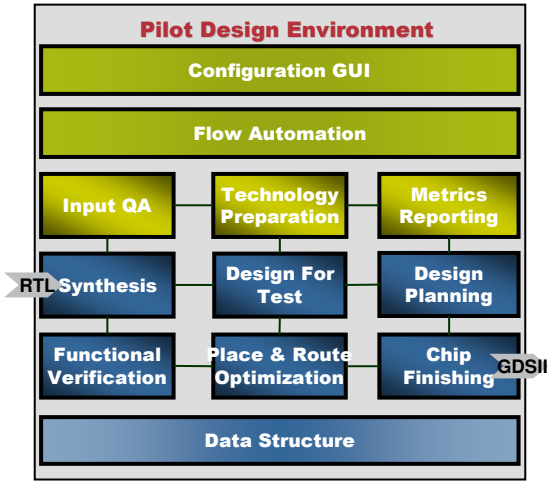
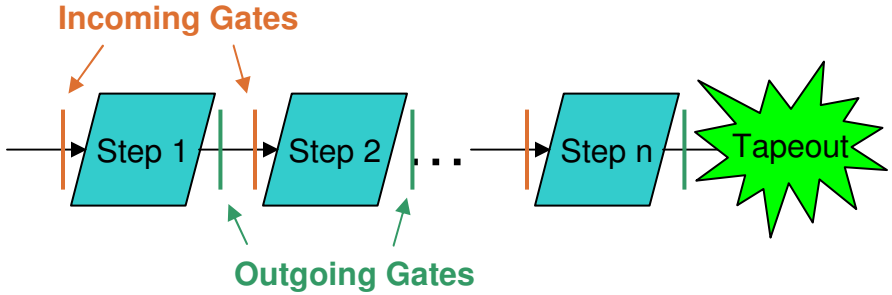
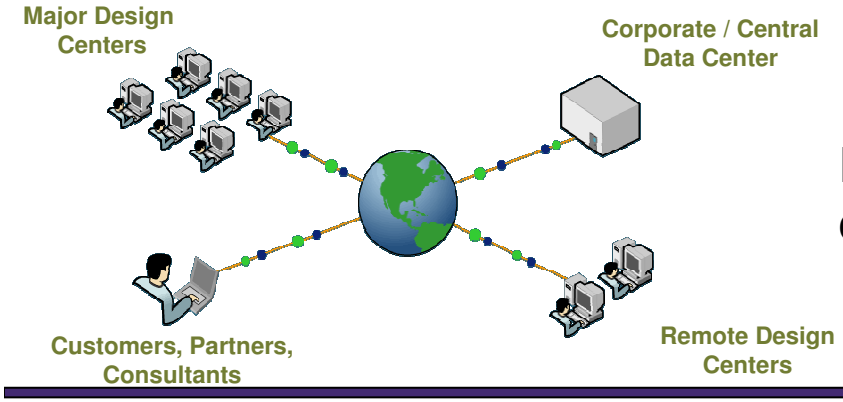
Global Technical Solutions



Pilot provides a mature, modular environment and flow to help maximize repeatability, efficiency, and productivity

Quality checks and reviews ensure successful execution of projects according to plans





DesignSphere compute infrastructure helps ensure worldwide team execution

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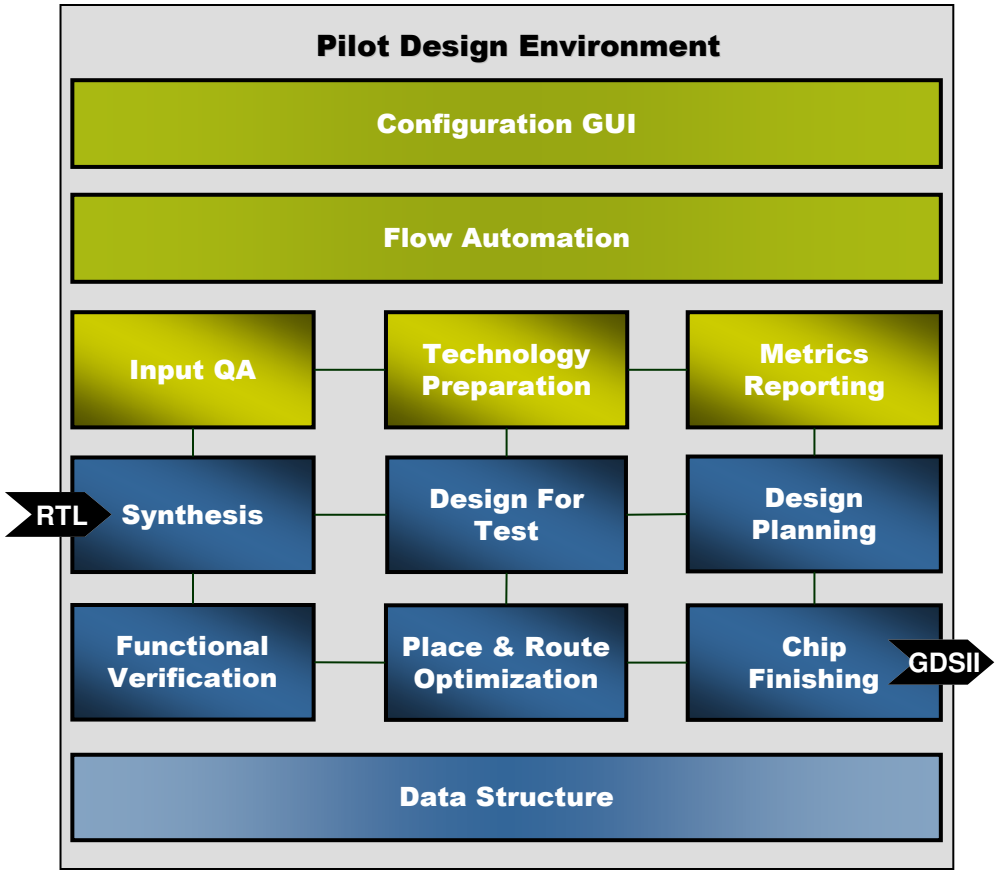
Pilot Design Environment Overview



- Open, ready-to-use, VDSM tested design system
  - Configurable for customer-specific environment
  - New utilities for IP & lib-QA, technology file preparation & metrics reporting
  - GUI for ease of flow setup
- Deployed to customers & used by Professional Services, WW
  - Enable consistent multi-site, multi-project IC development
- Updated & supported by Synopsys Professional Services

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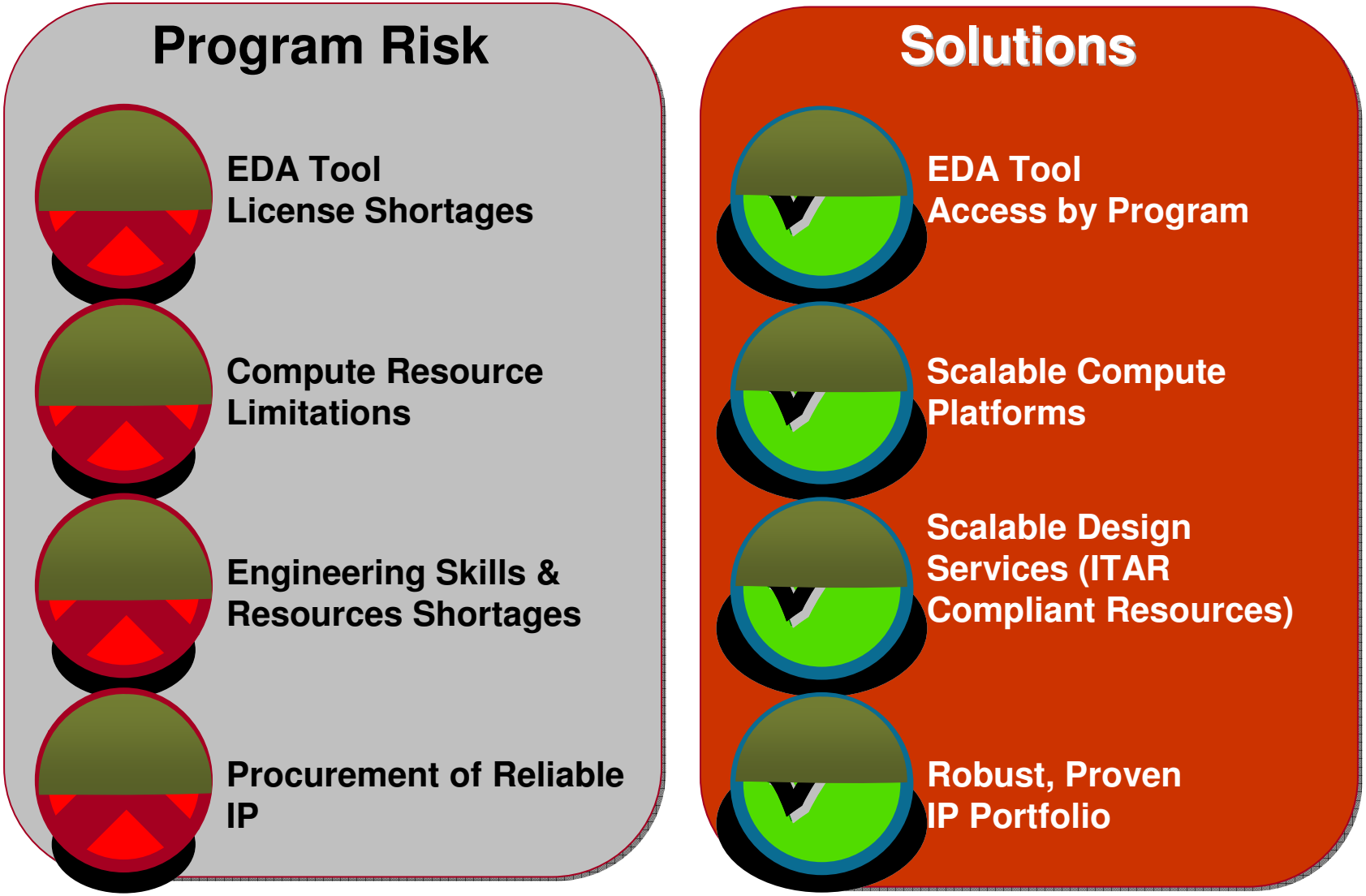
Solutions to Reduce Program Risk



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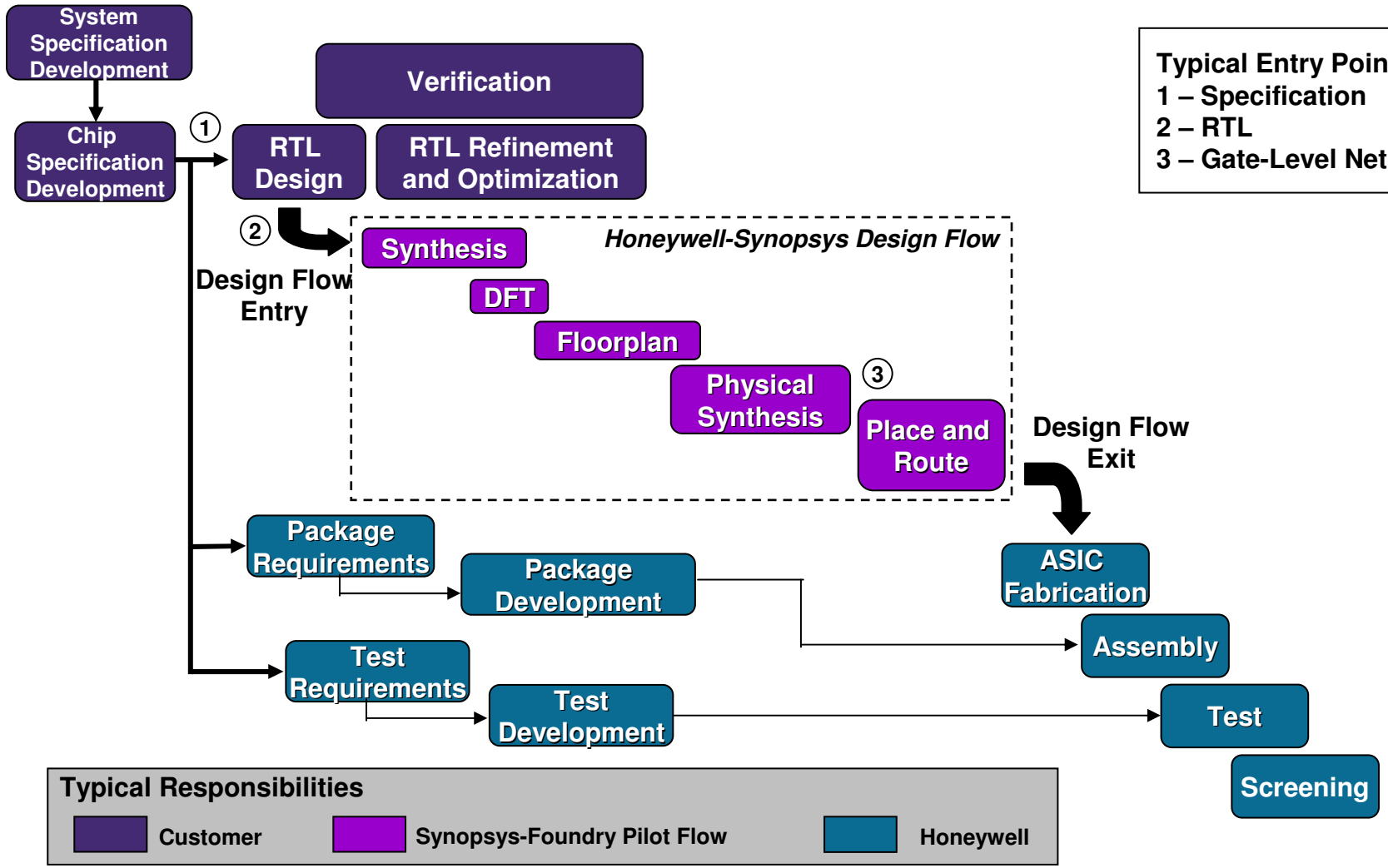
Honeywell/Synopsys Design Flow



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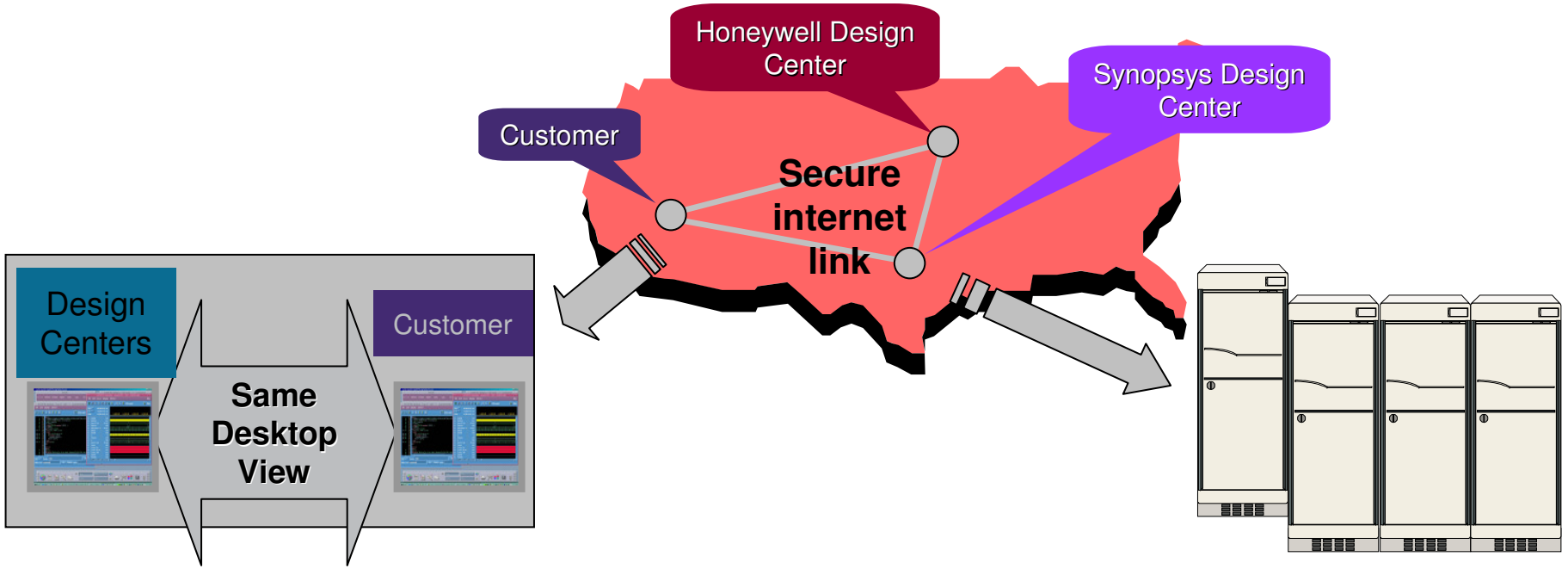
Design Collaboration Environment Scalable Infrastructure



- **Collaborative design infrastructure**
  - **Enables customer, Honeywell and Synopsys engineers to act as single design center**
  - **Use a common Pilot flow**
  - **On-demand availability of tool licenses**
  - **ITAR Compliant**

- Scalable data center
  - Server farm with 100's of CPU's
  - LSF based job launching for parallel computing
  - Regular back-ups
  - Physically secured and monitored 24x7x365

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