Yield Explorer

Design-Centric Yield Management

Overview

Nanometer node yield issues are dominated by design-process-test interactions, mandating cross-domain analyses to mitigate these issues rapidly. Yield Explorer brings yield relevant data from diverse sources such as the physical design flow, wafer manufacturing, and wafer and chip level testing into a single data bank. With the widest possible range of data at their disposal, users achieve unsurpassed clarity in root cause analysis when faced with systematic yield limiters. Yield Explorer achieves this with an order of magnitude advantage in analysis speed in the most complex of use cases—for example, 10X faster volume diagnostics analysis of ATPG output.

This significant analysis capability and speed advantage sets Yield Explorer in a class apart from previous yield management systems and enables, for the first time, true connectivity to EDA tools.

Yield Explorer Fully Addresses the Needs of Product and Test Engineering Teams

- Rapidly diagnose yield and performance issues with available fab, test and design data
- Accept any new types of data for ease in characterization and debug efforts
- Maximize learning from first silicon debug and minimize design re-spins
- Enable wide standardization of analysis methods through scripting and automation
- Manage the product across multiple wafer sources and test houses

Design At the Core of All Activities

A built-in layout viewer makes it easy to correlate any yield relevant information to physical design, e.g. failing cells to DRC flags or lithographic marginalities (Figure 1).
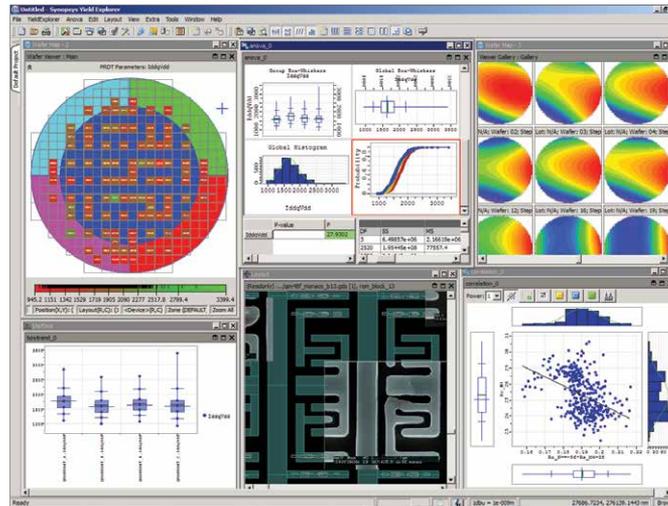

Figure 1: The versatile Yield Explorer client simultaneously manages a variety of yield data

Customization and end-User Control

Analysis routines are easily automated, and the application can be rapidly extended using built-in industry-standard scripting.

Rapid and Secure Data Access

Mobile and geographically distributed workforces can easily and actively participate in data-driven decision making.

Yield Explorer Benefits

- Improved turnaround time to find design, test and production problems (from weeks to hours)
- Quality of results (high accuracy of failure analysis candidate identification)
- Easy customization of recipes for each customers' unique requirements (editable in Tcl scripting environment)
- Open architecture and flexible interface (enables connectivity to existing customer databases)

Key Technical Features

- A full complement of statistical and data analysis tools along with wafer and test visualization capabilities
- Complex correlations across site-parametric, design, physical verification, simulation, product test and custom data sources
- Synchronized Component Architecture integrates all incoming data into a single, coherent analysis application
- Interactive use-case flow between the chart and spreadsheet windows to wafer maps to failing net overlays onto design
- Dynamically extendable data model to accept any number of custom data fields into the Yield Explorer database
- Platform neutral Analysis Client (Windows, Linux, UNIX) to allow all users to use the same application regardless of desktop computing environment

Typical Yield Explorer Use Case

One of the key decisions in solving yield issues on early silicon lots is to separate the random yield loss from systematic yield loss. Most often, random yield loss is controlled by fab defectivity and is handed over to the fab to rectify.

Systematic issues, however, need careful analysis by product and test engineers to understand the root cause of the failures leading to yield loss. Modern structural testing techniques like DFT diagnostics identify possible candidate cell occurrences in a given design that may have contributed to a given die failure.

Once the XY locations of failing cells and nets are overlaid on top of the physical layout an entire new set of possibilities is opened for analysis. For example, the identified cells are logical entities which are manifested in several layers of GDS file as physical entities. FEOL DRC flags within the XY coordinates of failing cell boundary provide one explanation for the observed failure, whereas BEOL DRC flags provide connections to failing nets.
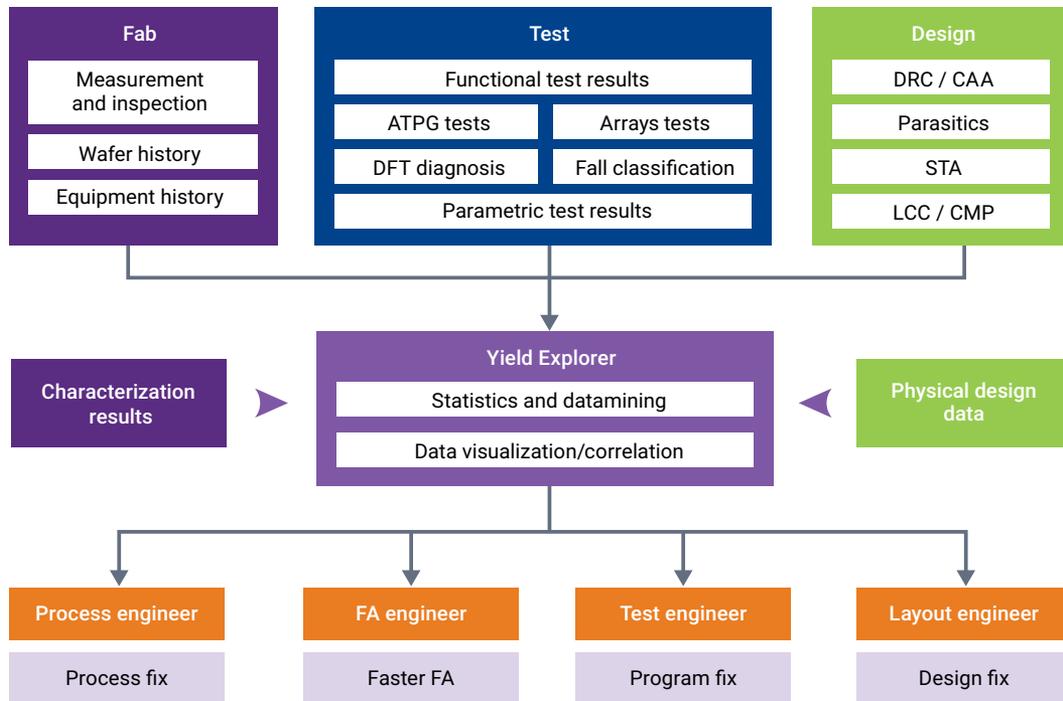

Figure 2: Yield Explorer collects data from fab, test and EDA domains to enable faster discovery of yield root-cause sources
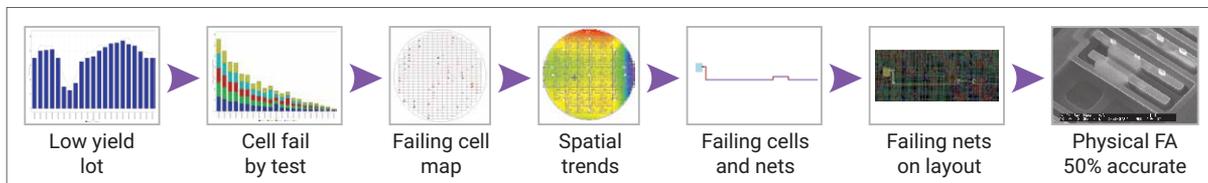

Figure 3A: Traditional diagnostics methods typically require 2-3 weeks to reach root cause—and with only about 50% accuracy

3
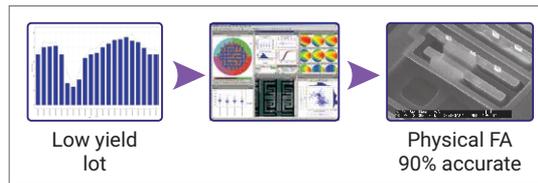
Figure 3B: With Yield Explorer, actual time to results, with 90% accuracy, was reduced to 2-3 days

Additional information about hotspots, as simulated and flagged through LRC or stress models, provides alternate explanations for cell failure.

By allowing the customer to do this in a single seamless system (Figure 2), Yield Explorer offers a tremendous time savings (Figure 3) over the manual movement of volumes of data between logical, electrical and physical domains.

Efficient and Effective Analysis

- Yield Explorer Assistants help users create more efficient analysis flows:
- Chart/Data Analysis Assistant
- Spreadsheet Assistant
- Data Selection Assistant
- DRC Assistant
- Rapid data extraction over Wide
- Area Networks
- Client Scripting using Tcl/Tk
- User actions recorded as analysis flows in Tcl script format

Additional Capabilities

- Application Developer's Kit (option)
- Provides access to Yield Explorer data to drive external applications
- Job Scheduler (option)
- Users can schedule specific jobs to run on a periodic basis in an automated manner

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.