TechTalk

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Synopsys Professional Services - Systems-Level Design Services - Wireless and Broadband Communications Domains

Rapidly increasing complexity of modern wireless and broadband applications require proven solutions for implementing new functionality. At the same time, shortening product lifecycles require that these products hit the market early with clear differentiation.

Helping designers meet these challenges, Synopsys Professional Services offers Turnkey Design Services specifically focused on wireless and broadband applications. Utilizing broad experience within these communications domains, Synopsys provides expertise where cutting-edge developers need it the most – in the design and architecture of the high-level system. Optionally, Synopsys Professional Services can then take on the full design implementation to netlist or GDSII.

The Systems-Level Design service develops the system architecture and specific algorithms for the customer's wireless or broadband application. Synopsys follows a disciplined design methodology and leverages extensive project management experience. Synopsys Professional Services offers expertise with highly-specialized systems-level design flows, along with expertise in RTL development, design reuse, logic/physical synthesis, functional verification and conformance verification (Figure 1).

From Concept through Executable Specification to Verified RTL

The Systems-Level Design service typically begins with the translation of a high-level product concept into a functional specification. With a functional system specification, Synopsys offers a wireless and broadband design service that delivers verified RTL. Optionally, the service can be extended to design integration, netlist sign-off or GDSII tape-out. The targeted implementations can range from an ASIC subsystem to complete chip sets.

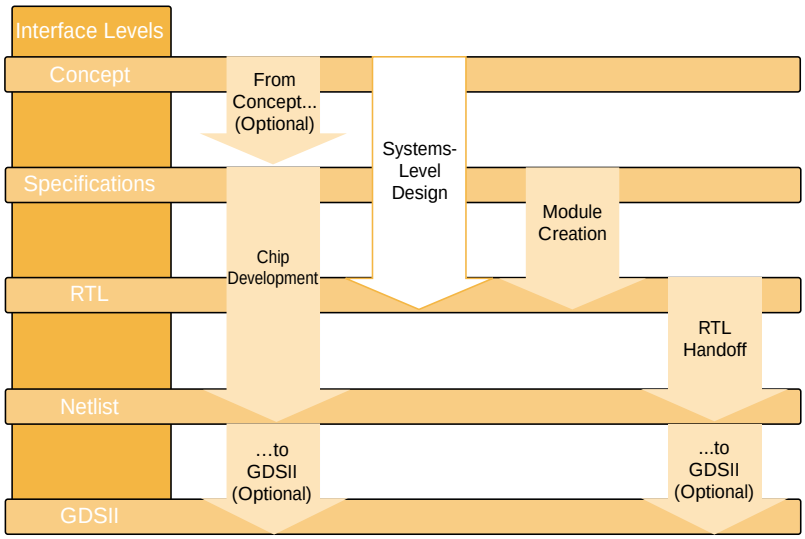


Figure 1: Portfolio of Synopsys Turnkey Design Services Offerings

The Synopsys design flow creates an executable specification to model the design functionality and then converts that model to RTL with complete functional verification. A systems-level design approach based on an executable specification allows for refinement of functionality without time-consuming RTL changes. This approach enables efficient system partitioning among multiple ASICs or among hardware and software. The executable specification also helps in optimizing the chip's architecture.

Refining and verifying the executable specification helps achieve a solid first-time-right specification. Functional changes during or after RTL design are sometimes unavoidable. In these situations, the executable specification offers a rapid way to verify the impact of the changes to the functionality and implementation before RTL redesign. This procedure avoids excessive iterations due to inefficient change processes.

Along with the wireless systems-level design, Synopsys executes functional and conformance verification. This is facilitated through the use of Synopsys' Wireless Reference Design Kits for applications such as EDGE and UMTS. These ensure compliance to industry standards and aid algorithm development and performance analysis.

The Synopsys Telecommunications Workbenches for standards such as ATM, SONET/SDH and IP are used for standards-based compliance verification, and testing of telecom functionality for broadband designs. Custom testbench models and test cases also support

design-specific functional verification. The chip-level verification suite is used at each step in the design flow from verifying the behavioral systems model to final chip level simulations.

Wireless Application Systems-Level Design

Because wireless physical-layer designs often include support for multi-standard, multi-rate functionality, they require expertise with wireless applications and signal processing as well as a cohesive design methodology.

The Synopsys design methodology for wireless transceivers accommodates the need for extensive signal-processing work that includes algorithm design and optimization. The defined algorithms are then included in the floating-point model that defines the design's entire datapath. This enables systems-level simulations such as evaluating receiver performance using the floating-point model along with realistic analog front-end and transmission channel models.

Synopsys Professional Services accelerates systems-level modeling with the use of behavioral building blocks such as modulators, filters, and converters. The hierarchical behavioral modeling results in reusable components for future projects and allows evaluation for different implementation architectures.

After the floating-point model is completely verified with systems-level simulations, Synopsys refines it to a fixed-point representation, creating a bit-true model of the design. While the fixed-point model can be verified with the same stimulus used on the floating-point model, the effects of finite word length, rounding and truncation must be verified to ensure that the system response does not change. Control structures such as processor interfaces and serial interfaces are also modeled with fixed-point representations.

In parallel with defining the design architecture, Synopsys further refines the fixed-point model to include the effects of the control flow. Additionally, our designers evaluate parallel versus sequential implementations for optimizing size or performance.

The resulting bit and cycle-true models enable co-simulation against the RTL design. Starting from the floating-point design, Synopsys creates a hierarchical model to match the design partitioning. This approach enables systematic bottom-up verification by replacing the behavioral blocks with their RTL counterparts—one by one—while co-simulating the RTL blocks.

Broadband Application Systems-Level Design

Synopsys' broadband Systems-Level Design service targets the development of NPUs for ATM and IP broadband applications with a methodology that begins with the creation of an executable specification. This approach allows for fast refinement of functionality without RTL changes. It also enables efficient system partitioning between hardware and software or among multiple ASICs.

Synopsys offers applications and standards expertise in a wide variety of communications systems including products utilizing ATM, SONET/SDH, PDH and IP protocols. Synopsys Professional Services also utilizes workbenches that verify the chip is functionally correct and conforms to the latest industry standards.

Referencing the functional specification, Synopsys creates an executable specification coded in SystemC™ or C++. The executable specification can cover a portion or all of the design. SystemC and C++ offer the ability to describe both hardware and software processes with the same language. Additionally, this high-level modeling facilitates reuse because the functionality modeled can be leveraged for next-generation designs, even if those designs require architectural changes. The Synopsys methodology also enables integration of customers' legacy IP in C/C++, RTL, VHDL™ or Verilog by using specific code wrappers that allow the execution of system simulations.

Once the functionality and standards conformance is verified with the functional model, Synopsys refines the functional model according to the chip architecture. Implementation-specific factors are added at this time. Adding the implementation details to the executable specification creates a model that is true to the final implementation and thus enables co-simulation against the final RTL code. The implementation-true model also allows the design's performance to be optimized through architectural refinements. The executable specification is designed to comply with the architecture of the final RTL design.

The design methodology based on executable specifications has proven to apply particularly well to applications that handle packet traffic, as in ATM traffic management or IP packet processing. Complex functionality such as IP packet header parsing must be verified

under conditions that are as realistic as possible. An executable specification serves as the basis for this realistic verification.

Design Implementation

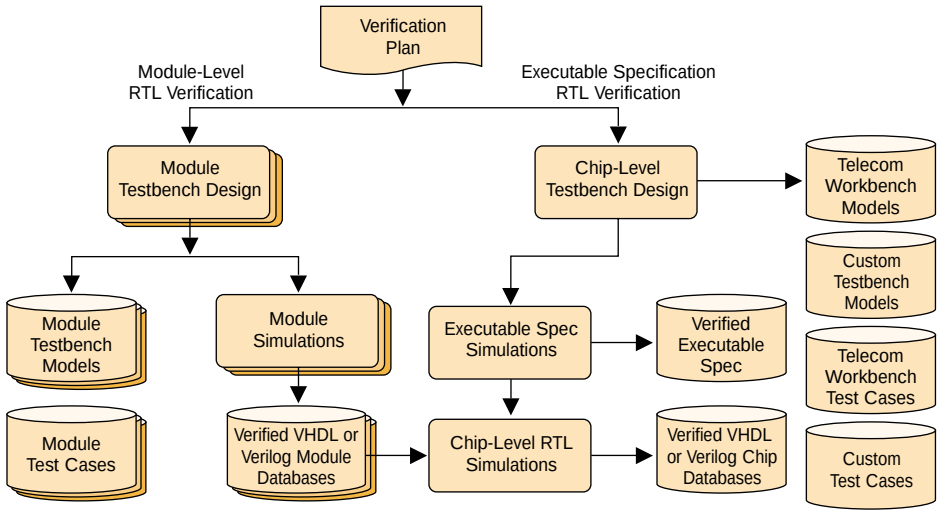
Synopsys refines the targeted architecture from the executable specification to a top-level HDL description with all the sub-block entities and their interconnections defined. Additionally, Synopsys defines the timing budgets for synthesis and static-timing analysis.

RTL design begins with micro-architecture design and proceeds to code development in either VHDL or Verilog. Synopsys can apply specialized tools such as Module Compiler™ for optimized datapath synthesis. When building the micro-architecture of the sub-blocks, Synopsys designers can utilize a variety of silicon-proven building blocks such as arithmetic structures.

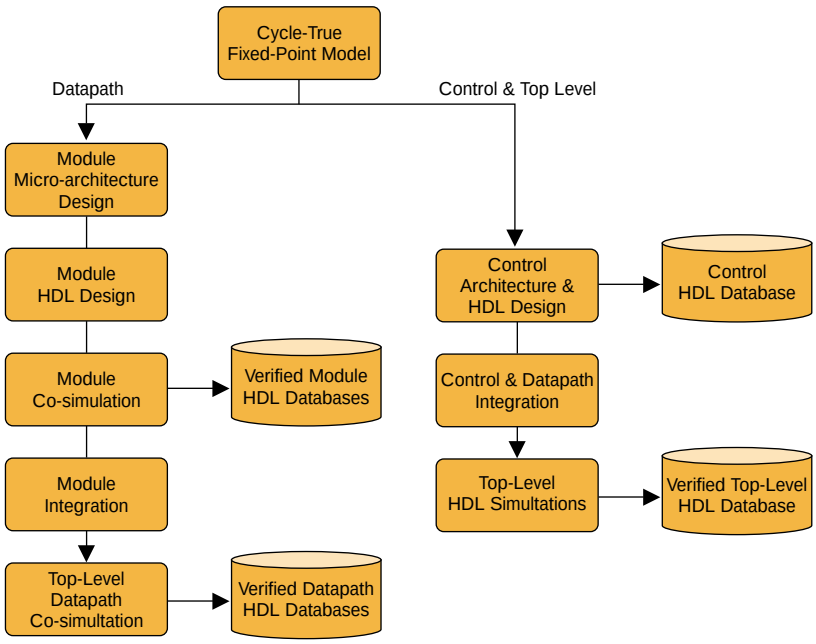
Along with the RTL design database, Synopsys delivers all the necessary synthesis scripts and timing constraint files. Synopsys also provides its customers the complete testbench environment. To ensure design reuse, Synopsys uses HDL checker tools to verify the design and coding against rule sets based on the Synopsys co-authored *Reuse Methodology Manual for System-On-A-Chip Designs*. Leveraging a disciplined design methodology results in highly reusable IP for follow-on projects.

Functional Verification

Functional verification is extremely important for the success of the chip. To shorten design time, Synopsys specifies and executes complete hierarchical functional verification in parallel with creating the functional



Figures 2: Broadband Hierarchical Functional Verification



Figures 3: Wireless Hierarchical RTL Design and Functional Verification

specification and design. The verification process includes systems-level verification of the executable specification and chip-level RTL, as well as separate module-level testbenches that support a hierarchical, bottom-up approach to RTL verification. The use of a hierarchical approach ensures good coverage and efficient execution (Figure 2 and 3).

Synopsys begins functional verification with the creation of a verification strategy that outlines the overall verification approach. The verification coverage and resulting design quality is managed by referencing the design requirement and selecting appropriate verification tools and methodologies. This includes simulation, coverage analysis, hardware/software co-verification, testbench automation, verification models and standards-based compliance verification. Referencing the functional specification and datasheet, Synopsys develops a detailed verification plan that contains descriptions of test cases and the chip- and module-level verification environments.

The testbench is comprised of automated stimulus generators and self-checking response analyzers controlled by the test-bench core, which executes the test cases. This automated testbench environment provides fast turnaround for regression tests. For broadband solutions, Synopsys designs all testbenches to be modular for reuse in future projects. Testbench structures and test cases are designed with VERA®, HDL or C/C++ along with support from Synopsys Telecommunications Workbenches. Synopsys analyzes simulation coverage when running both sub-block and module-level simulations and guides the verification process with the results by quickly creating additional tests for the corner cases left untested.

Documentation and Knowledge Transfer

Documentation is important for wireless and broadband product development. Synopsys provides a functional specification that serves as the primary reference for the executable modeling and functional verification. Along with the functional specification, Synopsys also provides a chip datasheet that describes physical characteristics, including full programming model and external interfaces. Additionally, Synopsys documents the architectural reference model for use in RTL design, providing descriptions of chip-level architecture and module interconnections among others.

When Synopsys refines and implements a design, knowledge transfer back to the customer's design team plays an important role in the design delivery process. This knowledge transfer minimizes their learning curve and ensures that a detailed under-standing of the executable specification and implemented RTL stays in-house.

Summary

Synopsys Professional Services has deep expertise and experience at the systems design level in two vertical market domains: wireless and broadband communications. Customers take advantage of this expertise to accelerate their product development and raise the skill level of their internal teams. Synopsys' design consultants are familiar with the latest wireless and broadband standards, enabling SoC developers to take on the dramatic increases in design complexity with confidence.

Pekka Leinonen
Synopsys Professional Services Technical Marketing Manager
leinonen@synopsys.com

http://www.synopsys.com/sps/wbc.html