

Synopsys Professional Services - Chip Development Turnkey Design Services

Getting complex systems-on-a-chip (SoC) designs from the concept stage to netlist or GDSII in a predictable and expedient way is always a challenge. Whether or not chip design is an in-house development activity, the requirements of today's SoCs demand a knowledgeable and proven partner to complete chips on spec and on time. Turnkey Design Services from Synopsys Professional Services offer SoC developers access to one of the industry's most skilled and experienced design organization for their critical projects (Figure 1).

Synopsys' Chip Development service takes the design from the functional specification (chip concept) to ASIC or GDSII sign-off. This includes the logic design and IP integration, as well as complete functional verification. Synopsys has multi-disciplined design teams that provide application knowledge and proven expertise in systems design, logical and physical synthesis, verification, design for test, and design for reuse. Synopsys uses advanced EDA tools and methodologies combined with experienced project management to offer a predictable schedule. And Synopsys'

time-to-market pressure and shrinking process geometries, the standards are continually evolving.

The best design methodology is dependent on the application, and even within a single SoC, several design methodologies can be used. For wireless SoCs, Synopsys can tailor a full solution from high-level concept for the transceiver using a COSSAP® or Co-Centric® System Studio-based executable specification that models the entire transceiver through floating- and fixed-point representations. For other IP, where non-standard, custom functionality is needed, a Synopsys design team works closely with the customer to address the differentiating features of the product through textual or executable specifications. Similar executable specification methodologies based on SystemC™ are utilized for broadband applications.

In the wireless and broadband domains, Synopsys has extensive expertise in the design and architecture of the system. Synopsys offers both Wireless and Broadband Systems-Level Design Services, which is explained in more detail in the next TechTalk article following this article. Because of the complex set of industry standards in these applications, verifying compliance is critical. Synopsys uses a portfolio of technologies that not only verifies that the chip is functionally correct, but also conforms to the latest industry standards.

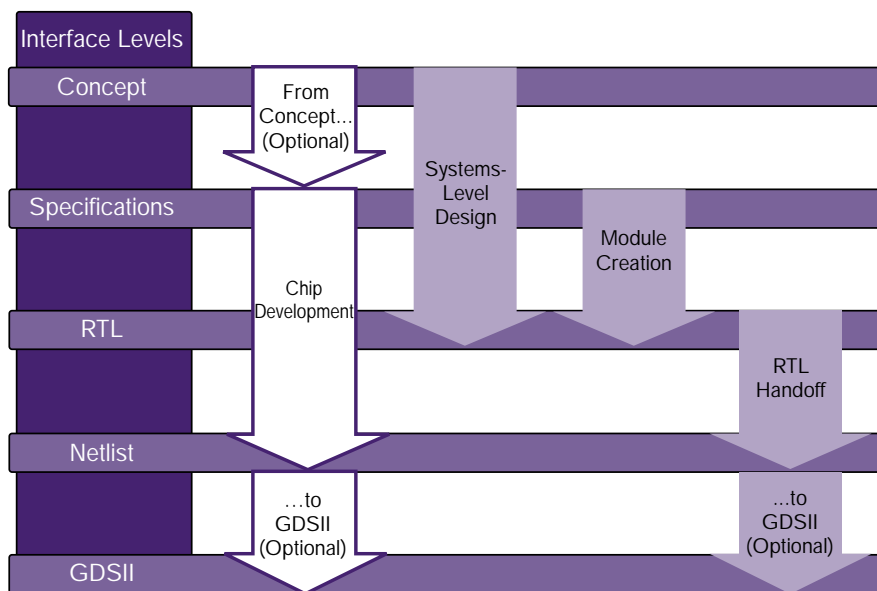


Figure 1: Portfolio of Synopsys Turnkey Design Services Offerings

Providing turnkey services that range from systems design through netlist handoff or GDSII tape-out, Synopsys takes on the responsibility for the design deliverables. The design work is typically completed in a Synopsys Professional Services' design center, where the engineering teams, latest tools, flows, and compute infrastructure are already in place for fast deployment.

design flows and methodologies are compatible with a wide variety of silicon manufacturers and technology providers.

Systems-Level Design

Among today's most challenging projects are the complex communications chips for advancing wireless and broadband applications. In addition to the standard

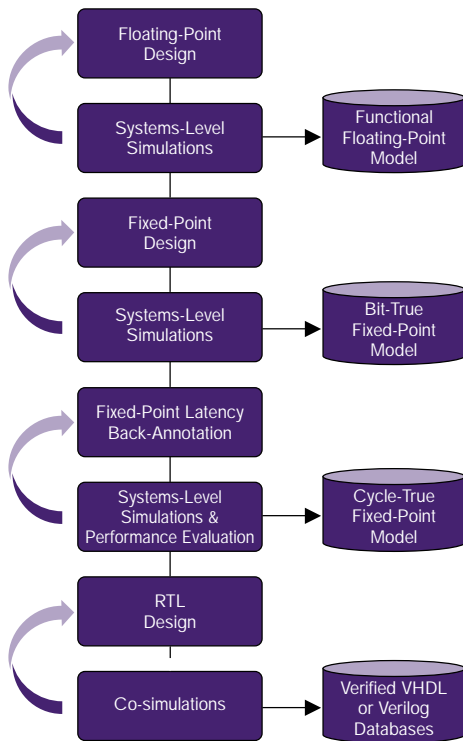


Figure 2: Wireless Systems-Level Design Flow Based on Executable Specification

RTL Design

Having the design specifications accurately defined before detailed design is the first milestone to predictable project delivery. This is one of the major benefits of using design outsourcing because both Synopsys and the customer's internal team combine to consider all aspects of the implementation even before design work begins. Time spent up front to make the chip specification as detailed and accurate as possible is time well spent – even the smallest scope change occurring late in the project can prevent tape-out on time (Figure 2).

RTL creation is done with VHDL™ or Verilog following design and coding against rule sets based on the Synopsys co-authored *Reuse Methodology Manual* for *System-On-A-Chip Designs*. For high-performance datapath-intensive designs, Synopsys can also apply Module Compiler™ for more optimized implementation. Synopsys' DesignWare® library provides an extensive resource of building block IP for accelerating the design creation.

Implementation

Design integration must be done in parallel to RTL design creation to ensure predictable and fast timing closure. Creating an initial floorplan, which includes at the architecture design phase the top-level interconnections and top-level IP entities with their respective gate count estimations, prevents surprises in late stages of the design cycle.

After the design is coded and the RTL is complete and verified, Synopsys moves quickly to netlist sign-off or to GDSII tape-out, depending on the customer's manufacturing model. Synopsys Professional Services' methodologies for physical synthesis and static-timing analysis reach rapid timing-closure faster by reducing iterations between logical and physical abstractions.

Synopsys begins the chip implementation by performing logic synthesis on the module (i.e., block-level) RTL. The synthesis is

guided by the chip-level timing budgets defined during the chip partitioning. For complex and high-speed SoC designs, Synopsys uses physical synthesis to create a placed-gates database using actual cell distance rather than wireload models for more accurate results.

Integration of IP from various sources is an important task in SoC design. Synopsys' designers have experience with a wide variety of industry-standard IP, including standards-based interfaces, microprocessor and microcontroller cores, memories and silicon libraries. If needed, Synopsys can evaluate the availability of suitable IP from sources internal and external to the customer.

The final floorplan is created with the gate counts of the synthesized module databases. Chip-level synthesis integrates the modules and IP blocks into a single chip-database for timing analysis and design for testability. Together with chip integration, the power distribution planning is also executed when targeting a COT manufacturing model or placed-gates ASIC sign-off. The power distribution planning follows specific guidelines from the chip manufacturer. The placed-gates planning using physical synthesis is followed by clock-tree synthesis to balance the clocking networks.

Synopsys has experience with a wide variety of vendors and technologies that contribute to a low-risk ASIC or COT implementation. In addition to a disciplined design approach, Synopsys Professional Services' experienced project managers provide focused management and reporting practices to ensure a predictable delivery schedule.

Functional Verification

Synopsys performs the complete functional verification in parallel to creating the design. By referencing the functional specification and datasheet, Synopsys develops a verification plan describing the testbenches and test cases for both module- and chip-level verification.

Synopsys' verification uses a hierarchical approach that ensures high coverage and effective execution. The coverage and resulting design quality is managed by referencing the functional specification and selecting the appropriate verification tools and methodologies. Depending on the requirements, Synopsys uses mixed-language simulation, coverage analysis, hardware/software co-verification, test-bench automation, and standards-based

compliance testing to ensure thorough verification of the design.

The process of functional verification is guided with the reports of coverage analysis. The corner cases left unverified after the first set of simulations are quickly identified and exercised with new test cases. With hierarchical verification methodology, the targeted module coverage enables well-verified sub-systems to be integrated at the top-level.

Synopsys creates testbenches with self-checking stimulus generators and response analyzers to be modular for future projects and for reusability between the module and chip-level verification. Testbench structures and test cases are designed with Synopsys VERA®, HDL or C/C++.

Sign-Off

For ASIC-manufactured implementations, Synopsys provides the verified netlist. Before the netlist sign-off, the design goes through the required ASIC vendor design flow and design rule checks. In the case of a timing-driven layout sign-off model, Synopsys provides the chip database together with the timing constraints to the ASIC vendor, who performs the layout and timing verifications, as well as any hard IP integration.

Working with the ASIC manufacturer for a traditional ASIC sign-off model, Synopsys performs post-layout timing analysis using back-annotated information from the ASIC vendor. If timing violations are detected, the chip database is re-optimized using in-place optimization before a new layout iteration. Once the design meets its timing and

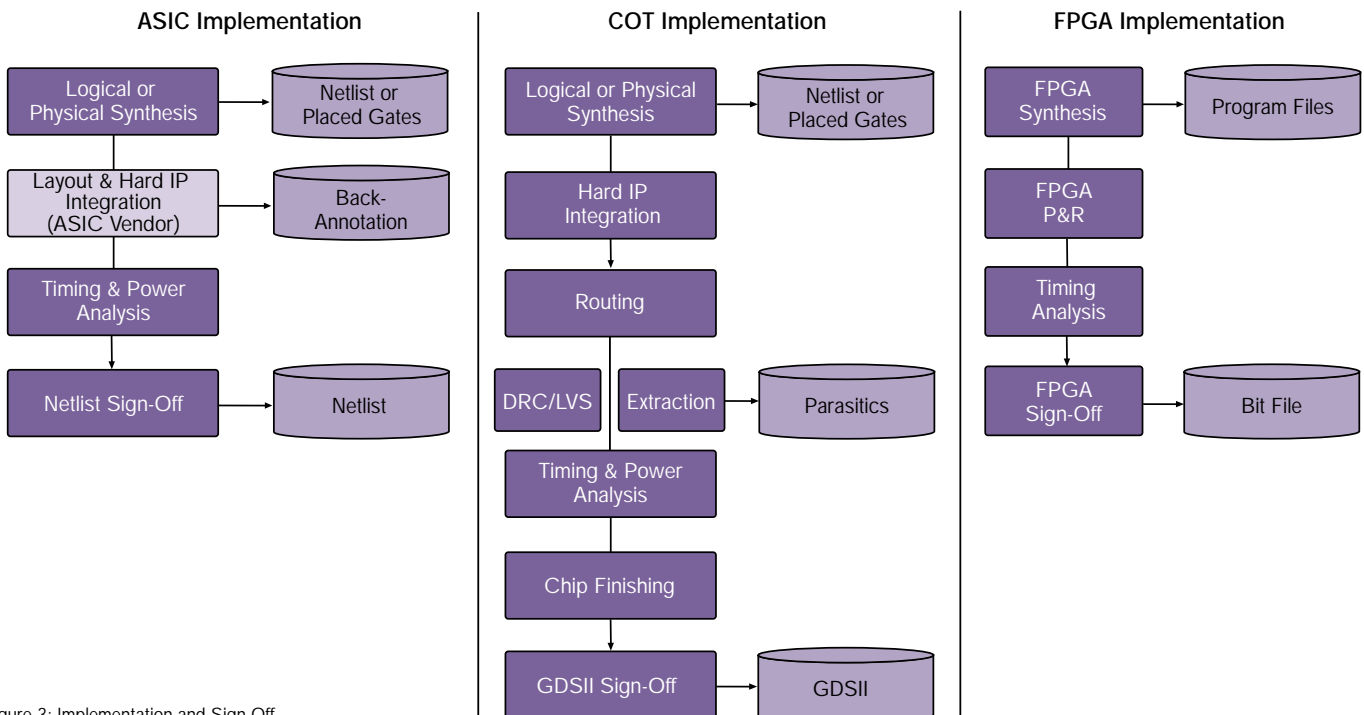


Figure 3: Implementation and Sign-Off

power requirements, Synopsys releases the netlist to the manufacturer.

To support COT manufacturing models, our design team will take the design from placed gates to GDSII, also integrating hard IP as applicable into the design. Synopsys performs the detailed routing and physical verification (DRC, LVS, and extraction), as well as a detailed timing and power analysis on the layout database. Once the database is fully verified to meet functional and performance criteria, Synopsys releases the GDSII to the foundry.

FPGA implementation is done using the FPGA vendor's place and route tool from the synthesized chip database. The place and route is guided with edited timing constraints initially defined for FPGA synthesis. The FPGA place and route tool extracts the bit file needed for the device configuration. Timing analysis is done utilizing the same tool, taking into account the additional delays caused by the placement and routing.

In case of minor timing violations after FPGA place and route, the FPGA synthesis and place and route are re-constrained and re-executed for more accurate results. If the design size and clock speed are pushing the capacity and performance limits of the FPGA, the design is carefully optimized in the chip architecture and RTL design phase taking into account the device specific FPGA architecture to ensure achieving the target performance (Figure 3).

Summary

Increasing size and complexity, advanced manufacturing processes, and compressing market windows make systems-on-a-chip development more challenging than ever. Offering a full range of Turnkey Design Services from concept to GDSII, Synopsys Professional Services is a strategic resource that complements and extends the existing capabilities of SoC developers.

Synopsys can take a high-level specification and deliver a verified netlist or GDSII tape-out. Synopsys gives customers access to a design team with extensive experience at every phase of the SoC development cycle.

Synopsys Professional Services has expertise in specification development, RTL design, design reuse, logical and physical synthesis, physical design, and functional verification. Synopsys offers a portfolio of Turnkey Design Services to augment and complement existing development capability, providing greater flexibility in managing challenging design programs.

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