Synopsys Professional Services – Consulting Design Services

Overview

Because the complexity of modern systems-on-a-chip (SoC) designs need expertise in a wide variety of design disciplines, developers often find it challenging to maintain the complete set of required specialties in-house. For SoC developers in which chip design is an important core competency, Synopsys Professional Services offers Consulting Design Services to help improve their internal design capabilities and accelerate their key projects. With an insourcing engagement model, Synopsys designers work as members of the customer's development team, sharing expertise and experience to solve design bottlenecks such as timing closure and functional verification (Figure 1). Synopsys addresses the immediate design project and deploys the latest flows and methodologies to help with future ones.

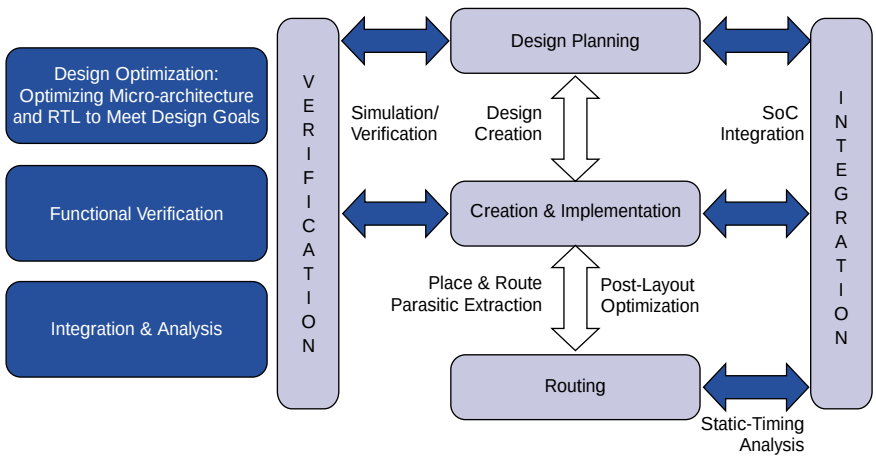

Figure 1: Consulting Design Services Address Design Bottlenecks

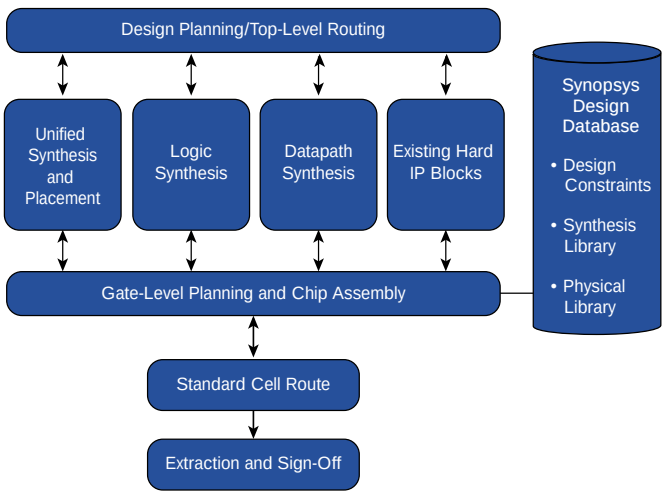

Figure 2: Synopsys' Chip-Level Physical Synthesis Solution

Synopsys Professional Services offers Consulting Design Services that can be summarized as three complementary services: Design Optimization, Functional Verification, and Integration and Analysis. Our customers bring in-house one or all of these services to augment their existing development capability. This article provides a brief introduction of each of these service offerings.

Design Optimization

Iterations between layout and synthesis for complex SoCs can result in a lengthy design cycle as designers try to resolve the physical effects on the logical design. The core of the Synopsys physical synthesis flow is Physical Compiler™, which unifies synthesis and placement to provide rapid timing closure from RTL to placed gates. Synopsys Professional Services' Design Optimization helps take a customer's most crucial IP block through the physical synthesis-based flow to expedite timing closure (Figure 2).

The Design Optimization service focuses on solving the implementation bottlenecks that arise in validating all of the design inputs and constraints; optimizing the design to meet timing, test and placement constraints; and incorporating the design module into the full-chip implementation. This service brings together knowledge of design and advanced methodologies. Synopsys Professional Services has acquired these skills through experience optimizing a wide variety of complex designs ranging from graphics engines to vector CPUs.

Synopsys Professional Services engages with customers at a variety of levels. In the most straightforward type of engagement, Synopsys focuses on optimizing the most crucial block of a design by taking it through the physical synthesis flow. To enable this flow, the Synopsys Professional Services team evaluates the block's area, timing and pin-placement constraints, as well as assumptions about the block's design characteristics.

The Synopsys team also derives and updates the design's block-level budgets from chip-level constraints. These updated block constraints are then used to optimize the design. Evaluating the block-level budget using chip-level constraints is an important step in the process of meeting the overall design objectives.

Chip-level partitioning for both timing and function are necessary to achieve timing closure for complex designs. Synopsys defines issues that the design team can address to improve timing closure, partitioning and budget refinement. The Design Optimization service also provides a production-ready flow that simplifies the adoption of physical synthesis. Synopsys takes care to transfer knowledge of the physical synthesis methodology in conjunction with the optimization of the critical blocks. Synopsys can continue with other crucial blocks or the entire chip design. Multiple Synopsys teams can optimize blocks in parallel, and perform block integration and timing analysis.

Synopsys can also optimize the design to meet power or area constraints. Early in the project cycle, Synopsys provides services to optimize the design's micro-architecture to meet project goals. Synopsys' services can be extended to include implementation of the remaining SoC design blocks, as well as the resolution of chip-level bottlenecks all the way through GDSII tape-out if required.

Functional Verification

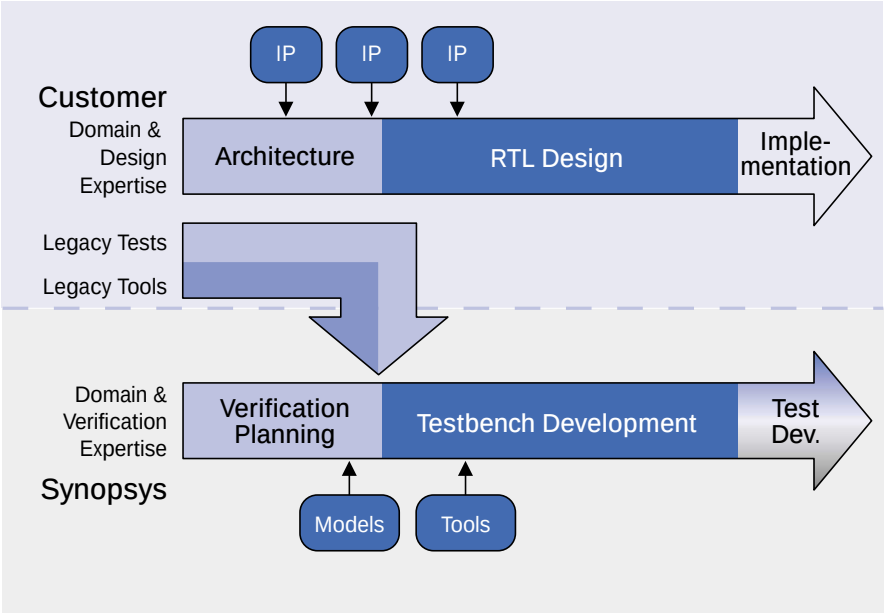

Figure 3: In parallel with the design activity, Synopsys prepares and executes a detailed verification plan, including testbenches.

Verification has grown disproportionately to the size of the design, accounting for up to 70 percent of the total development effort. Consequently, the need for specialized verification knowledge has steadily become more important. Synopsys' Functional Verification service uses the latest verification technology, including random stimulus-generation, functional-coverage monitoring, and self-checking testbenches.

The verification effort runs in parallel with the design effort (Figure 3). A verification team from Synopsys applies a proven, structured verification methodology that includes development of a detailed verification plan as well as automated test-benches for execution. As the RTL is completed, a large set of automated tests is ready to identify problems. This concurrent approach substantially reduces chip-development time.

The first task in the Functional Verification service is to create a detailed verification plan. This plan serves as the blueprint for the execution phase, in which the test-benches and tests will be implemented. The verification plan documents the technical understanding between the design and verification teams, and how the SoC verification task will be addressed.

Next, Synopsys executes the documented plan. Synopsys focuses on developing the testbenches and overall verification infrastructure including models, monitors,

stimulus generators and hardware/software integration. Testing from the block-level to the systems-level is performed. The Synopsys verification strategy enables the generation of many vectors in a short time, so that first-round tests achieve a high rate of coverage. While the design team fixes bugs and reapplies the tests, the verification team works with the designers to define additional tests that address corner cases to achieve the optimum coverage.

Traditional approaches put 20 percent of the verification work into developing test-benches and 80 percent into developing tests. The Synopsys methodology reverses this arrangement by putting 80 percent of the effort into developing testbench facilities that automate test generation. By bringing greater automation to testing, more tests can be created in less time, and test results require little manual analysis.

As a significant element in the Synopsys verification methodology, Synopsys designs self-checking testbenches to be interface-centric, viewing the RTL as a black box. Drivers exercise the RTL that constitutes the device under test (DUT), while protocol monitors watch the bus and report illegal behavior and data values. Additional monitors provide support for debugging and coverage evaluations. A software driver, developed by Synopsys or the customer's design team, configures the DUT and runs low-level software. This interface-centric approach works well with the typical SoC design, in which IP blocks interact through well-defined interfaces.

Test coverage is another key part of the Synopsys verification methodology. Monitoring stimulus coverage provides information on the quality of the stimulus generated. The Synopsys CoverMeter tool measures how well the tests exercise the HDL code. Functional coverage is checked using the OpenVera™ language, user-defined expressions in CoverMeter and additional assertions written in RTL. These methods increase the effectiveness of random testing and complement the interface-centric approach by exposing the internal structures of the DUT to testing. These checks cover design intent to make sure that all corner cases are exercised, provide feedback that allows refinement of the random stimulus being generated, and serve as debug aids by catching problems as they occur.

Integration and Analysis

The quality of IP building blocks for SoCs has a profound impact on the downstream device timing. Integration and Analysis service eases timing closure by qualifying IP and associated timing models. This allows the design team to establish realistic timing budgets from the beginning of the design project, which then serves as the basis for timing analysis throughout the project.

Synopsys Professional Services addresses timing issues with services that include SoC integration and the application of static-timing analysis (STA) and formal verification. The typical Integration and Analysis engagement has three basic phases (Figure 4).

In the first phase, the Synopsys team gathers the static verification requirements and builds a specific environment for the project. Synopsys also captures and validates the design's top-level timing constraints and views, and performs a preliminary analysis using the available timing models. This preliminary analysis clarifies the timing challenges in the design. At the end of this phase, the design team examines results, validates the timing exceptions (false and multi-cycle paths), and defines the course of action for the remainder of the engagement.

Synopsys then identifies issues to be resolved to complete chip assembly. An inventory is taken of the available physical data and the different timing models required for full-chip analysis. Using pre-route design data, Synopsys performs initial STA and formal analysis. Block-level budgets are developed using the top-level constraints from phase one, and these are refined with

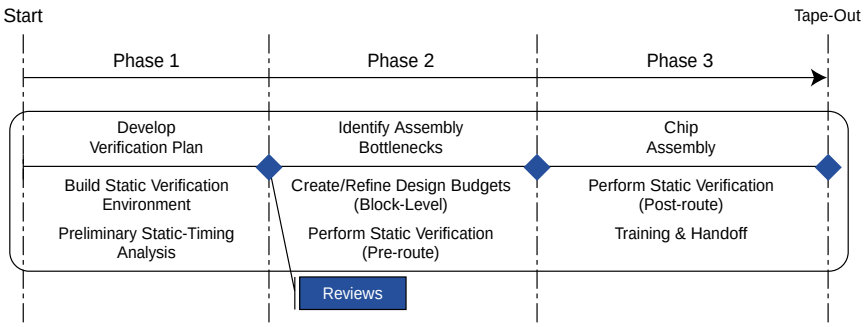

Figure 4: Typical Integration and Analysis Engagement

successive improvements in the block-level design. At the end of this phase, the design team can review the chip-level assembly issues, review the pre-route timing results, and refine timing exceptions.

Finally, Synopsys works with the design and layout teams to resolve the bottlenecks in the chip assembly process identified in phase two. Using the post-route netlist and parasitics, Synopsys performs STA and formal analysis to ensure the design database is ready for sign-off. Synopsys uses the static verification environment to train the design team and hand off the environment for follow-on design projects (Figure 5).
Synopsys also evaluates the available timing views, timing data, and the sources of the timing data. If multiple timing models are involved (transistor, gate and RTL models, for example), Synopsys ensures that the related tools interact appropriately. The test resources are organized to account for different functional modes of the SoC, such as normal operation and power-down modes.

Synopsys delivers the analysis environment in the form of Tcl scripts, directories, functional constraints, timing budgets, and training for the customer's design team. Synopsys will perform pre-layout and post-layout STA along with formal verification as needed. You receive both a verified design and a STA-based timing verification environment that can be adapted for use in other projects.

Integration considerations must be comprehended in the earliest phases of the design process—not just at the end—as they have a significant influence on SoC timing closure. This is especially important when integrating third-party IP blocks and memories. Synopsys considers the effects of the physical implementation in the early phases of RTL development and integration, helping floorplan the design, complete the top-level route, and validate the top-level constraints.

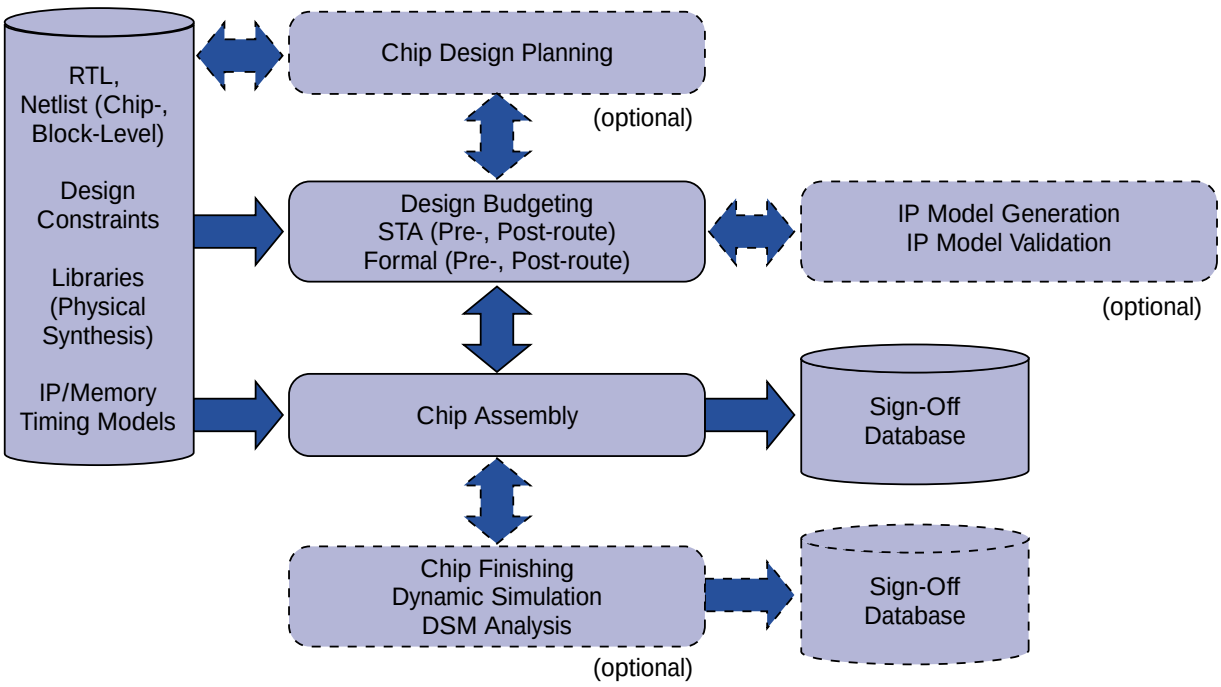

Figure 5: Chip Integration and Analysis Flow

Because analog and memory content is prevalent in modern SoCs, timing analysis cannot be limited to static verification, which only addresses the digital portion of the chip. Final sign-off can include mixed-signal simulation and analysis. Synopsys extends its static verification methodology to incorporate dynamic simulation and deep submicron analysis, analyzing the design for crosstalk and bringing the analog and memory models into chip-level simulations to perform targeted tests on them.

Summary

Building a multi-disciplinary development team with all the expertise to develop today's SoCs can challenge even the most sophisticated design organizations. Synopsys Professional Services provides both Turnkey and Consulting Design Services to meet our customers' unique challenges. Consulting Design Services is performed as members of the customer's development team, to not only accelerate their current key project but to also transfer valuable knowledge in design and design methods that impact future programs. Consulting Design Services consists of three complementary services: Design Optimization, Functional Verification, and Integration and Analysis.

Design Optimization service gives designers access to highly qualified teams for optimizing complex designs with physical synthesis to achieve rapid timing closure on their most critical blocks. Functional Verification service provides expertise with the most difficult verification challenges across a broad range of applications. Integration and Analysis service eases timing closure by qualifying IP and associated timing models. Whether a customer chooses to engage in one or all of these consulting services, Synopsys Professional Services helps ensure design success today and prepares the customer's design team for future success.

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http://www.synopsys.com/sps/cds.html