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Successfully Deploying Soft IP through Efficient Core Hardening and Modeling

By Jonathan Young and Pekka Leinonen, Synopsys Professional Services



Jonathan Young

For designers who want to take a quick and accurate route from RTL to GDSII consider this service solution for implementing ARM® soft cores from Synopsys Professional Services



Pekka Leinonen

Developers of system-on-chip (SoC) devices are turning to sources of ‘star IP’ for microprocessor and DSP core solutions. For IP suppliers and semiconductor vendors, a quick and accurate route to implementation from a soft IP representation is desirable.

Synopsys Professional Services’ Jonathan Young, design center manager, and Pekka Leinonen, technical marketing manager, outline a robust methodology developed in collaboration with ARM for “hardening” soft IP cores, which takes into account the qualities of complex soft IP.

Commercially available star IP is a key enabler for design reuse. SoC designs depend on the successful integration of several star IP blocks. The almost universal presence of the embedded microprocessor in SoC design-starts demonstrates the critical importance of star IP in the semiconductor value chain.

Deploying Soft Star IP Soft IP offers flexibility in being portable between different silicon processes and, being synthesizable, is compatible with the ASIC design flow. The IP integrator is looking for the ability to quickly assimilate, customize and integrate the soft IP, and of course do so in a manner that meets the system performance specification. That requires an efficient methodology for hardening the IP to new process technologies, as outlined in Figure 1.

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WEB LINKS

- [Synopsys Professional Services – Core Hardening](#)
- [ARM946E-S](#)

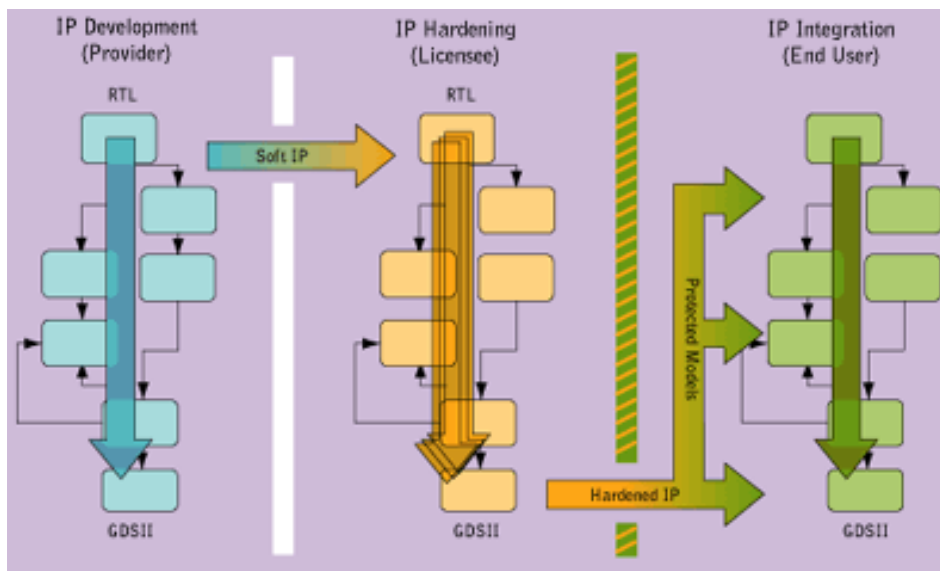


Figure 1. Soft IP Deployment

The relative merits of soft and hard forms of IP are well documented. Soft IP offers greater flexibility in being portable between different silicon processes and, if delivered as RTL, usually enables certain design parameters to be easily changed. Being synthesizable, soft IP is compatible with the ASIC design flow. The SoC design can therefore be optimized for a specific silicon process and performance target. The pre-hardened core carries less risk for the integrator. The performance characteristics are known in advance, and the designer is usually able to better predict the integration effort required. Hard IP is not as easy to port between different processes as soft IP.

Predictability IP Implementation

Typically, the semiconductor vendor or IP licensee will want to add value and differentiate the hardened core. This may mean taking advantage of features in their silicon process to differentiate the core for low power or performance during the hardening process. Ideally, the methodology should be automated to enable high productivity and repeatability. Moreover, it should be easy to use and learn and provide access to ASIC designers without specialist back-end design knowledge. To support integration with an ASIC flow, the hardening process must provide accurate models at appropriate levels of abstraction. A methodology that supports hardening independent of the design parameters or target process will ultimately offer a better return on investment because it will be reused for different IP and porting to other silicon processes.

Synopsys Professional Services has Experience, Expertise in Advanced Design Methodology

Synopsys Professional Services has expertise and experience in advanced design methodologies. Recently, Synopsys worked with ARM to create a reference methodology to support the hardening and deployment of ARM cores within the SoC development process.

ARM-Synopsys Reference Methodology enables an ARM soft IP integrator to customize, implement, characterize and deploy ARM's soft IP efficiently. The key motivation is the delivery of a proven route to silicon that consistently provides optimal hard IP both predictably and

deterministically. The output from the design flow is a validated GDSII database with functional, timing, test and physical models. The final hard IP should be easy to integrate into the final design. And of course, the hardening process should maintain the integrity of the design. This means that no architectural changes—not even minor RTL modifications—are allowed.

Methodology

The key steps in the core hardening reference methodology are the following:

Core Configuration. As well as setting the parameters enabled by the IP creator, configuring the core in the case of a microprocessor may also include customization of cache memory or selecting manufacturing test options, and other configuration options specific to the processor core.

Core Planning

The core planning process—critical for meeting the design's performance requirements—starts with positioning the major components: core, cache memories and I/O, for example. This initial floorplan is refined when the result of the initial logic synthesis run is known.

Core Synthesis. The reference methodology contains scripts to guide the synthesis process for a specific soft core. The scripts capture the synthesis strategy based on detailed design knowledge that the IP creators have. The scripts are critical in automating the hardening process and create an optimized implementation of the core. Because changing the IP architecture is not an option, the required clock speed must be achieved through physical design alone. Physical synthesis, which provides for timing-driven placement within the synthesis process, offers the best way of achieving timing closure for fixed IP.

Modeling

There are several requirements for modeling hardened soft IP. Often, the IP creator wishes to protect the IP by obfuscating detail within the implementation. Therefore, the models must have built-in security. Alternatively, the front-end models provided to the integrator may consist of 'black-box' representations suitable for functional and timing simulation purposes. Using consistent models throughout the design process helps to reduce inaccuracies and makes the design flow more predictable. Design language and simulator independence are also important factors in considering alternative model technologies.

The ARM-Synopsys Reference Methodology makes the same timing view available to logic synthesis, physical synthesis, static-timing analysis and place and route. This is made possible by extracting a sign-off quality-timing model using Synopsys' PrimeTime® static-timing analysis tool. At a functional level, the Synopsys family of model compilers for Verilog, VHDL and C code (VMC™, VhMC, CMC) provide protection against reverse engineering by compilation into binary object code.

This Reference Methodology has been deployed and proven effective. For example, Synopsys Professional Services has successfully completed a project for ARM to harden an implementation of the ARM946E-S™ core. This project targeted a TSMC 0.18-micron process for the ARM Foundry Program.

In this example, the implementation had to meet a specific target clock frequency of 160MHz, as well as provide reduced power and area figures compared with previous hardenings. Synopsys' Professional Services UK Design Center applied the core hardening Reference Methodology and achieved the specified implementation objectives. In addition to delivering a GDSII database, timing, physical and test models were also delivered to enable the ARM946E-S to be deployed in the chosen process.

ARM-Synopsys Joint Development Advances Hardening of Soft IP Cores

The joint development of the ARM-Synopsys Reference Methodology has greatly advanced a robust framework for hardening ARM soft IP cores. Synopsys Professional Services has experience and expertise in design hardening projects involving complex, high-performance star IP and provides consulting and design services to developers looking for an efficient and proven route to silicon.

Tools used in the Design Hardening Reference Methodology for the ARM946E-S are the following:

Clock Gating	Power Compiler™
RTL to Gates	Design Compiler™
Gates to Placed Gates	Physical Compiler™
Scan Insertion and reordering	Physical Compiler
Clock tree synthesis and routing	Apollo II™
Static Verification	PrimeTime and Formality®
Signal Integrity Analysis	PrimeTime-SI
Power Analysis and Optimization	Power Compiler/VCS™
IR Drop Analysis	Astro-Rail
Design Verification – LPE/DRC/LVS	Star-RCXT™/Hercules™
ATPG	TetraMAX®

Core Hardening Service

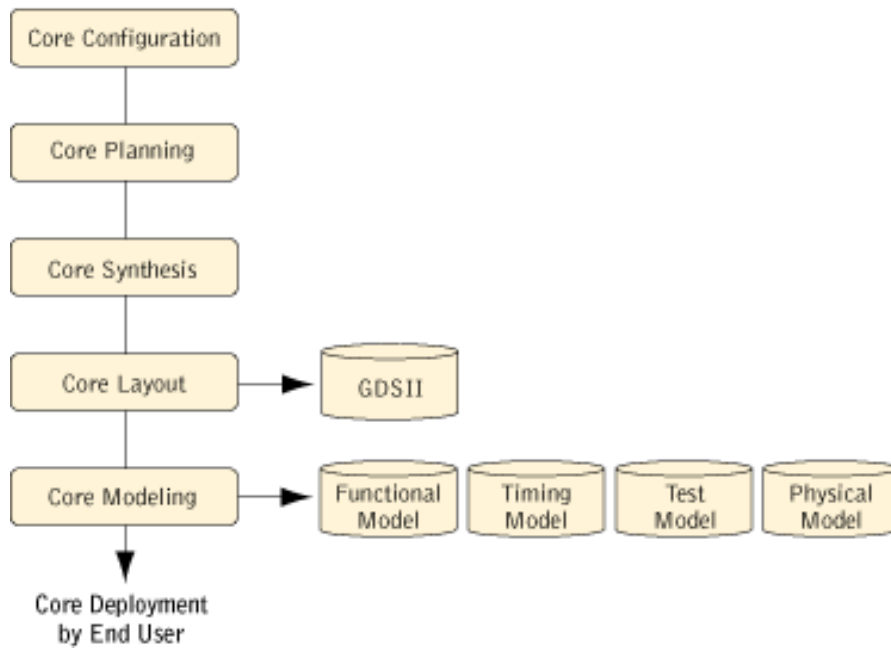


Figure 2. Major Steps in the Hardening Process

Pekka Leinonen is currently technical marketing manager with Synopsys Professional Services. During his career at Synopsys, Leinonen has worked in engineering roles in digital ASIC design projects and design flow development. He holds an M.S. in electrical engineering from Tampere University of Technology, Finland

Jonathan Young holds the position of senior manager, Regional Design Center with Synopsys Professional Services. With 15 years experience in the ASIC industry Young has held positions with Sony Semiconductor (Europe) and Texas Instruments Limited prior to joining Synopsys in 2000. He holds a B.S. in electrical and electronic engineering from the University of Reading, UK.