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Telecom Design Verification Challenges

Vincent Thibault -- *Electronic News*, 11/26/2001

Today, Telecom Designs deal with packet management, especially Internet protocol (IP) packet management. From the access market (mobile communication, xDSL and modem) up to the core network (optical transport), the common factor driving communications designs is the convergence of data and voice traffic over IP packet transmission.

This is especially true in the networking segment where system-on-a-chip (SOC) designs are integrated in all functions of the OSI physical layer dealing with bit transport up to the OSI network layer dealing with IP packet routing. This trend, especially for embedded applications, is moving more and more to the upper OSI layers that directly manage the application.

Telecom designs are complex SOCs. They provide network access to consumer electronic devices or to communication systems. Whatever the network interface, the networks carry information through encapsulated IP packets.

Mobile communications, access systems, and more generically, local-loop systems carry IP packets all the way up to the metropolitan area network (MAN) access point. LANs carry information with native IP packet technology for data via Ethernet. These two categories of systems (local-loop systems and LAN) handle the user-network interfaces encapsulating the information coming from the application into IP packets. This means that local loop systems and LAN play a key role in end-user services. They have the critical function of qualifying and identifying the service that the end-user is requesting from the network. Using different solutions, from allocated resources (similar to switching technology) to differentiated services embedded in the IP packet overhead information, the network access system identifies the quality of service (QOS) that the application requires.

Transporting the IP packets from node to node or from router to router, the MAN and core network transport systems have multiple network interfaces coming from network upgrades, a result of the recent technology evolution. These systems support PDH, ATM and SONET/SDH transmission technologies. Their basic functions address the first two layers of the OSI stack (physical and data-link layer) and, as a result, deal with increasing performance demands in terms of bandwidth and processing (optical framers include complex error detection and correction mechanisms such as CRC or FEC).

On the other hand, LAN and local-loop systems are more and more frequently involved in the upper OSI layer support (network layer or transport layer). This tends to introduce packet-based store-and-forward architectures in order to replace the existing synchronous circuit-switching architectures. It simplifies the clocking scheme, but parsing, classification, encapsulation, forwarding and routing of IP packets of variable lengths and types demand more processing. The

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increasing number of flows and classes supporting dedicated service agreements makes the management of the QOS the emerging issue.

To meet this challenge, system providers must struggle with complex queuing and scheduling algorithms involving all the resources of the system. This implies the use of architectures capable of intense processing and the storage of a large amount of data at wire speed, which increases system cost and engineering effort.

In profiling the telecom design, you could describe it as having at least one, but more often several network interfaces (modem, xDSL, TDM, PDH, ATM and SONET/SDH), and one or two large microprocessor interfaces. The new challenge in telecom design is clearly the QOS support and its underlying system resource interactions.

Verification is the bottleneck of design development. It is usually the most expensive and the most critical phase of development. Often verification makes up 60 percent or more of the time spent in design and is never exhaustively completed. The goal of verification is to reach the expected level of coverage (the level of confidence) with the minimum impact on the design development cycle (the market window and the cost). These issues are even more critical for designs in the fast-moving telecom market that require a strong verification methodology.

The first step of such a methodology is the assessment of the required test cases to be executed in order to achieve maximum functional coverage. It produces the verification plan, which must contain the detailed test cases to verify the design features. It must also take into account the available tools and models that the test cases require.

The second step is to develop stimuli generators and response analyzers in other words, functional models. This effort might be the step that takes the longest time when no reusable models exist. Telecom designs have multiple network interfaces, which require the development of several sets of stimuli generators and response analyzers.

The last step of the methodology is the integration of all the models. In this final step, choosing the right verification environment is extremely important. The verification environment the verification platform should be flexible enough to easily instantiate all required models while providing the level of control and observability required.

What differentiates the telecom design today is QOS performance. An integrated verification platform plays a key role in simulating real traffic and real interactions between verification models.

Interactivity capability between all models used to verify telecom designs is a key feature for QOS verification. Clearly, the interaction between the microprocessor interface model (providing access into the design registers) and either a generator or analyzer model is needed. This allows dynamic reconfiguration of the design and the models and allows the verification of a route look-up table reconfiguration. Interactivity also provides the capability to verify the critical parameter of the packet loss ratio (or dropped packet ratio). This test case involves interaction between the packet transmitter and packet receiver in order to correlate the received packet stream at the egress interface with the transmitted packet stream at the ingress interface.

Most of the scenarios used for QOS verification simulate real traffic in order to stimulate classifier or scheduler functions. This implies that the packet stream at the egress port must be checked for header information compliance and data payload integrity. A self-checking capability and functional models are other key features of a telecom verification platform. The consistency of the packet header information coupled with the class of service and the requested QOS performance are the features to verify.

The verification of today's telecom designs needs a proven methodology, a library of compliant telecom models and a flexible verification platform providing interactivity and a self-checking capability to perform QOS test cases.

Author Information

Vincent Thibault is a product marketing manager for Mountain View, Calif.-based Synopsys Inc.'s professional services' broadband products.

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