

Search


for:

Search key industry sites for:

Powered by e-inSITE and
GoogleYou are here > [Home](#) > Article[Home](#) | [Archives](#) | [Yearbook](#) | [Events](#) | [Part search](#)

Sections

- [News Analysis](#)
- [Business & Finance](#)
- [Semiconductors](#)
- [DSP/Mixed Signal](#)
- [Communications](#)
- [Convergence](#)
- [Capital Equipment](#)
- [Classifieds](#)
- [Test & Measurement](#)
- [Design Strategies](#)
- [Semiconductor IP](#)
- [Distribution](#)
- [Supply Chain Management](#)
- [Packaging](#)
- [Components](#)

 Click for a **FREE**
Print subscription
[Print-friendly version](#) [Email this story to a friend](#) 

Foundries Rise, But Not COT

*Vendors swing to ASIC houses for help in 0.13-micron designs*By Gale Morrison and Tom Murphy -- *Electronic News*, 10/8/2001

San Jose The semiconductor industry is embracing the foundry model more whole-heartedly than ever. But an interesting thing is happening on the way to tape-outs for the 0.13-micron process node.

Fabless companies are increasingly realizing that the customer-owned tooling (COT) model that arose alongside the foundries is simply too expensive and too complex. They are turning to services companies, they are going back to the ASIC houses and they are starting to work with the new hybrid of the two: fabless ASIC.

In the 80s and the early 90s, ASIC houses defined themselves. These were companies that worked separately from the system companies even if they sometimes shared a corporate parent needing the chips. LSI Logic, NEC, IBM, Texas Instruments, Toshiba, and a few others became giants making money on the business of meticulously designing these absolutely non-commodity parts, fabricating them as well, and getting them packaged.

But big kids can be bullies. Executives trying to get chips from them say the ASIC companies their suppliers they were paying wielded their monopoly arrogantly and locked customers into their process, their timeline and their considerable expense.

Customers, especially smaller companies looking to carve out a living with some key design wins and grow from there but also big companies battling for every last penny of their margins, became frustrated. Foundries saw this opportunity and started offering just manufacturing to those who could bring a GDS-II tape. EDA companies had been pumping massive R&D into commercial place and route tools for ASICs, which fabless companies realized they could use to do the back-end of design themselves. And they did just that. COT, customer-owned tooling, became three of EDA's favorite words. By the end of the 90s, fabless companies in PC graphics and broadband networking two extremely demanding, high volume applications rode this wave away from the ASIC companies to Wall Street accolades.

But, as you've heard over and over for the last month, everything has changed. Or at least, *is* changing. 0.13-micron design is requiring a massive EDA re-tooling. The software tools for physical synthesis and deep sub-micron analysis to feed into it are easily a \$5 million investment, and finding and paying a talented design engineering team to do it, easily another \$10 million. Those figures are per year, and it's certainly not that the software and manpower is overvalued. If anything, they come dirt cheap, considering the task at hand. Don't forget the millions for the intellectual property, the photomask sets with sub-wavelength



ST10 16-Bit MCU

for high-end
automotive and
industrial applications
flash versions
available.



Register!

ElectronicNews Today

Register to receive the day's hottest headlines delivered directly to your desktop.

[Register](#)

Tools & Services

- [Archives](#)
- [Research Highlights](#)
- [Yearbook](#)
- [Careers](#)

[Contribute](#)

Inside ENews

[Contact Us](#)

[Media Kit](#)

[Subscriptions](#)

Powered By



Capital Equipment Purchasing Study

Cahners Research identifies trends in equipment buying.

[Click here to view the Powerpoint presentation.](#)

Electronics Group Distribution Supplement

[Click here to view the Acrobat file.](#)

lithography engineering built-in and don't forget to double that bill since the advanced packaging these chips require cost as much as the chip.

All of this is driving some companies back to the ASIC houses.

"The tide is starting to change," said Bryan Lewis, principal analyst with Gartner Dataquest in San Jose. "Many companies six months ago thought they could go directly to the foundries and eliminate the ASIC companies. Recent comments from companies show that they are returning back to ASIC companies because the risk and overhead were too high to eliminate them," he said.

Broadband networking, with the incredible demands that fiber-fueled, wire speed packet processing brings to it, is first and foremost where this can be true.

"(S)ome of the hot networking companies are going to back to the (ASIC model) future," said Anjan (A.J.) Sen, former president of PulseCore Semiconductor and former executive vice president and founder of eSilicon Corp. of Santa Clara, Calif. "They've got 0.13-micron, ten million transistor designs and when you are pushing that envelope, you really need to go back to IBM. If you are bleeding-edge and pushing that envelope, there are very few vice presidents of engineering who will not go with the security of an IBM.

"That's basically how IBM has built its reputation," said Sen, who has been an ASIC and a foundry customer in his thirteen years in the business.

IBM builds all of AMCC's communications parts, and it is building the 10Gbit/sec. networking part due out from EZChip of Israel, to name two companies which might logically be with the foundries. Big Blue has a huge client list of networking and advanced graphics fabless customers. NEC Electronics Inc. of Santa Clara is building a highly advanced switch fabric part from Erlang Technology Inc. of St. Louis. Texas Instruments Inc. of Dallas is building the 10Gbit/sec. ASIC that Network Elements Inc. of Beaverton, Ore., needs. LSI Logic's tagline these days is communication, communication, communication.

Silicon Access Networks Inc. of San Jose, another hot team with \$100 million in venture capital to play with, is sticking with Taiwan Semiconductor Manufacturing Co. Ltd., the world's largest foundry, even though it's been an intense year learning that embedded SRAM at 0.13-micron would win out over the original embedded DRAM at 0.18-micron plan.

It is not unusual for a fabless company to seek out an ASIC house first as it gets its first design implemented in silicon, said Michael Buehler-Garcia, vice president of EDA for No. 3 foundry Chartered Semiconductor Manufacturing Ltd. of Singapore. Those companies require a higher amount of design services on the front end than what foundries usually provide. Of course, those services also come with a price, he noted, which ultimately translates into system costs.

Chartered doesn't see this as a threat to its business model, Buehler-Garcia said. Rather, they see it as further evidence that outsourcing is becoming more and more commonplace. If a NPU company contracts with Agere Systems Inc., for example, the silicon is usually spun at Chartered anyway. A company like Broadcom Corp. started out getting their ASICs made at IDMs. But as soon as they got market momentum and more engineers, they turned to the foundries.

Certainly, the foundry model works and it's not going away. LSI Logic and National Semiconductor completed contracts around 0.13-micron capacity at TSMC just this year, the foundry's U.S. spokesman Chuck Byers points out. But it's becoming clear that the engineering tasks the chip design, the mask sets, the



Anjan Sen, former president of PulseCore Semiconductor and former executive vice president and founder of eSilicon Corp.

test and packaging at the high end today are becoming the domain of large, established companies, and those who can pay for them.

"Customers want to write a check and get their chips," said Naveed Sherwani, general manager of Intel Corp.'s Microelectronics Services business, which is working closely with Synopsys' Professional Services unit. "We believe that there are two things to consider: these companies, ASIC customers, need to save money and they need to save opportunity.

"We are reducing their risk. First of all, if you are going to do just one or two chips a year, setting up a team, paying for the tools, setting up the supply-chain management for just a couple of chips is a huge set-up. For smaller companies, that are going to do only a few chips a year, this is a very large expense," said Sherwani. "If you are going to do just one chip with TSMC, time and time again there are things you forgot in tape-out&That's a very important aspect from a start-up point of view. They need an experienced team which does that alone, as their life."



Naveed Sherwani,
Intel's
Microelectronics
Services

[Print-friendly version](#)



[Email this story to a friend](#)



[About Us](#) | [Advertise](#) | [Register/Log In](#) | [Subscriptions](#)

© 2002 [Cahners Business Information](#)

Use of this website is subject to its [terms of use](#).

[Privacy Policy](#)