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Intel ASIC unit to focus on comms chips

By [Anthony Cataldo](#)
[EE Times](#)

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SANTA CLARA, Calif. — Intel Corp. has formally launched a full-fledged ASIC division focused on communications chips, and is building a network of third-party intellectual-property suppliers to support the effort. Intel will also work with the professional services division of Synopsys Inc. to assist customers in the early design and product-specification steps.

Unlike traditional ASIC suppliers, Intel will rely on foundries, reserving its own production capacity for its bread-and-butter microprocessors and other standard products.

Intel's adoption of the "fabless ASIC" model, perhaps surprising for a company with its own vaunted process technology, builds on the long-term trend in the semiconductor industry toward foundries, commercially available intellectual property (IP) cores and EDA tools, and other services.

Despite the industry downturn, Intel said it is sanguine about the long-term prospects for communications-related ICs, noting that ASICs and application-specific chips now account for 41 percent of the communications market.

Yet Intel appears to be carefully choosing its battles. Naveed Sherwani, general manager of Intel Microelectronics Services, said Intel's ASIC initiative will focus on system-bandwidth killers rather than devices for commodity products. That means the company is less likely to build cell-phone baseband chips than chips for wireless basestations.

Intel was also vague about which of its microprocessor cores it will make available to its ASIC customers. It's a key question because of potential conflicts of interest with Intel's Xscale processor division. The ARM-based Xscale embedded processor targets both consumer electronics and networking applications.

Intel's microelectronics division has 16-, 32- and 64-bit cores available today, but so far the company has declined to disclose which microarchitectures it is using for ASIC designs. Intel officials said there's no readily available litmus test when it comes to which processors it will support.

"If there's a specific need a customer has, I don't think we'd say 'No we're not going to work with that piece of IP,' " said Craig Peterson, general manager of Intel's Microelectronics Services division (Hillsboro, Ore.). "I wouldn't leave it as an open checkbook, but I would say we are open to working through those types of needs with them."

Intel's latest ASIC play comes 12 years after its last effort to penetrate the ASIC market, which was eventually aborted because of capacity conflicts with microprocessors. The difference now is that Intel can draw from a plentiful supply of foundry capacity and intellectual property on the market, essentially allowing it to focus on design.

"I think we know the [fabless ASIC] concept is evolutionary and is happening whether we like it or not," said analyst Will Strauss, president of Forward Concepts. "The real surprise is that Intel is doing it. Maybe Intel wants to get out in front of a parade that's already begun."



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Strauss said it's likely that Intel will offer its Xscale processor and Frio DSP cores to ASIC customers, saying "those are the two things people covet most outside the Pentium and Itanium." But he said it's understandable that Intel probably would not want to build mobile-handset chip sets for outside customers, because the company is trying to sell its own standard chip set for that market.

Some observers expressed surprise that Intel would outsource its manufacturing and wondered whether the decision was an opportunistic move to fulfill foundry wafer commitments. In fact, over the past two years Intel has been quietly working with the major foundries to prepare for the new service and is working with an undisclosed number of customers, such as Transwitch.

Lesson learned

The use of foundries should avoid conflicts when its microprocessor customers are on allocation, a lesson the company learned in its last attempt in the ASIC market. "It's a bad value proposition to tell customers that we would have to cut their microprocessor allocation so we could build ASICs for them," said Peterson.

Even if capacity gets tight at foundries, Intel should have the clout to ensure a steady supply of wafers. "If you're TSMC [foundry Taiwan Semiconductor Manufacturing Co.], you probably don't want to tick off Intel. I would suspect they would have an easier time than most getting silicon," said Jordan Selburn, principal analyst with iSuppli (San Jose, Calif.).

Moreover, foundries offer a wide spectrum of process and transistor options, spanning from low power to high performance. "At 0.13 micron, there's an unprecedented number of new processes to create optimization," Peterson said.

Focusing on custom and application-specific ICs for the communications infrastructure is a better fit for Intel's high-speed CMOS, some said. "Cell phones require more processing power but not the clock speeds that are going to trigger an Intel-like approach," Selburn said. "Intel may be able to "ing some hard-won expertise. A Pentium runs much faster than any ASIC does."

Partner power

But fast digital logic won't be enough. Intel's intellectual-property allies say the chip giant has a keen interest in acquiring analog and mixed-signal capabilities to enable fast interfaces. "By the end of the fourth quarter, they're looking at doing things like Serdes and Xaui with an Infiniband interface," said Darla Berkel, senior marketing manager for Nurlogic Design Inc., one of Intel's partners.

Intel has also forged an agreement with analog and mixed-signal IP specialist Leda Systems, which will provide both Intel-approved off-the-shelf IP and, in some cases, custom circuits.

"The digital design is moving into a frequency range where the effects need to be taken care of in analog," said Zarko Nozica, vice president of applications engineering for Leda.

What Intel promises to "ing to the table is a design methodology that borrows tricks from its microprocessor design group, such as yield analysis. Intel also said it will be quick to address problem areas for deep-submicron design. Those include signal integrity (starting at the 0.18-micron design node) and leakage current, soft errors and in-die variation (at 0.13 micron and below).

The company claims it has developed a rigorous, four-stage hierarchical design flow after netlist handoff that can be monitored through a secure Web site. "In every phase, you have a strict checklist you meet, and in this way you have a predictable march toward tapeout," general manager Sherwani said. "In the case of an engineering change order, you can predict how long it will take and decide on the trade-offs."

For customers who need design assistance prior to place and route, Intel will work with Synopsys Professional Services, which has worked with Intel on a design flow for a smooth transition from synthesis to place and route. "We have a joint design-flow and management team, so to the customer it appears as one team rather than two companies," Sherwani said.

Fabless cachet

While fabless ASIC companies are not new, Intel's endorsement gives the concept the cachet it once lacked. "At one level, I'm flattered," said Jack Harding, president and chief executive officer of eSilicon Corp. (Santa Clara), a startup with a business model similar to Intel's microelectronics services group. "They'll make it a market, and we'll just be bidding against them."

If Intel can skillfully coordinate its manufacturing and IP suppliers, its move into ASICs could upset the balance of power among the larger ASIC suppliers that have to bear fixed manufacturing costs, driving up the minimum production volumes they will need to remain profitable.

The company said the flexibility of its business model will ensure that it can make money while being price-competitive with other ASIC companies. "Where they may not have margins with

[nonrecurring engineering charges], we do have margins," Peterson said.








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