

DesignWare IP and System-Level Solutions Portfolio

Synopsys DesignWare® intellectual property (IP) provides designers with a broad portfolio of digital IP cores, verification IP, and hardened mixed-signal PHYs. When combined with our large investment in design for reuse and verification methodology, certification, silicon validation, and comprehensive worldwide technical support, DesignWare IP gives hardware designers a faster and lower risk path to chip success.

Synopsys system-level solutions include tools and virtual platforms that connect hardware and software development flows for leading system-on-chip (SoC) platforms.

DesignWare IP Portfolio

DesignWare Library

Better designs start with better IP. That's why more than 25,000 designers trust the Synopsys DesignWare Library comprehensive portfolio of synthesizable IP, verification IP, and foundry libraries to quickly implement and verify challenging ASICs, SoCs, and FPGAs. The DesignWare Library significantly improves design quality of results with best-in-class datapath technology and is tightly integrated with the Synopsys Galaxy™ and Discovery™ Platforms. The DesignWare Library contains the principal intellectual property ingredients for design and verification. A single license gives designers access to all of the implementation and verification IP in the Library.

- Improves quality of results (QoR) for datapath intensive designs
- AMBA™ 2.0 AHB™/APB and AMBA 3 AXI™ implementation IP and verification IP
- Microcontrollers (8051, 6811)
- Complete memory portfolio (SDRAM controller, BIST, building blocks and over 10,000 memory models)
- Verification IP for standard bus protocols (PCI Express®, USB 1.1/2.0/OTG, SATA, Ethernet, and more)
- Foundry Libraries (TSMC, Chartered, and Tower)
- Design views of popular Star IP processors, and DSP cores
- Broad verification IP

DesignWare Verification IP

The DesignWare suite provides the industry's broadest portfolio of standards-based verification IP (VIP). It easily integrates into SystemVerilog, Verilog, VHDL and OpenVera® testbenches and supports all major simulators. DesignWare verification IP combines with DesignWare implementation IP and hardened PHYs to provide complete solutions for today's most popular connectivity protocols. It is fully configurable to support integration testing of DesignWare IP cores in a wide variety of applications. It also supports the constrained-random, coverage-driven methodology defined in the *Verification Methodology Manual (VMM) for SystemVerilog*, and is an integral part of the Synopsys Discovery Platform.

- Supports all major simulators and enables up to 5X faster runtime performance when used with the Synopsys VCS® solution
- Includes extensive testbench examples for rapid creation of integration tests
- DesignWare verification IP is available for PCI Express, USB 1.1/2.0/OTG, AMBA 2.0 AHB/APB, AMBA 3 AXI, Ethernet 10/100/1G/10G, SATA, PCI, PCI-X®, I2C, and Serial I/O protocols, as well as more than 10,000 memory models

DesignWare verification IP is available in the DesignWare Library, VCS Verification Library and as stand-alone suites.

DesignWare Digital Cores

Synopsys delivers silicon-proven digital connectivity IP for the world's most recognized products including consumer products such as game consoles, digital cameras, set-top boxes and HDTV, computing and storage equipment such as servers, printers, PCs and hard disk drives, communication and networking equipment such as switches, routers, network processors, and line cards. Provided as synthesizable RTL source code, these cores enable our customers to design innovative, cost-effective SoCs and embedded systems.

- Industry's first Wireless USB IP based on the certified wireless USB specification from the USB-IF
- Most complete and certified wired USB IP
- Leading supplier of PCI Express, including both Gen I and Gen II
- Comprehensive 10/100 Ethernet, Gigabit and 10 Gigabit Ethernet IP
- Power optimized storage solutions for SD, MMC, CE-ATA and SATA
- Automated IP assembly and reuse tools for integrating IP into an SoC
- Complete solutions for PCI Express, USB and SATA including digital controllers, PHYs, and verification IP

DesignWare Mixed-Signal IP

With Synopsys, designers have access to a wide range of high-performance, compliant and silicon proven mixed-signal PHY IP for the PCI Express, SATA, XAUI, and USB protocols. Combined with a suite of I/O libraries, which include DDR and DDR2 interfaces, the DesignWare mixed-signal IP (MSIP) portfolio allows designers to quickly and efficiently integrate high-performance interfaces into their next-generation SoCs. Adopted in many high-volume consumer applications, these high yielding MSIP are ported to over 30 different processes from 180 nanometer (nm) to 65-nm.

- Fully compliant PCI Express, SATA and XAUI PHYs supporting all lane configurations from x1 to x16
- High-performance architecture provides low area and up to half the power consumption of other solutions in the market today
- High-performing, robust designs, exceeding compliance requirements, with excellent margin. Built for seamless SoC integration
- Advanced built-in diagnostics, yield tuning, and test capabilities
- Complemented by a full suite of digital controllers and verification IP to enable complete SoC integration

DesignWare Star IP

Synopsys has maximized the power of partnership to deliver unique opportunities to design engineers who use the DesignWare Library or VCS Verification Library. Through the Star IP program, these designers can now evaluate and design using high-performance, high-value IP from industry-leading Star IP providers such as IBM, Infineon, MIPS, and Philips—right at their desktop. Each microprocessor has an AMBA AHB interface for compatibility with the DesignWare AMBA on-chip bus solution and other AMBA-based DesignWare IP, providing complete plug-and-play microprocessor subsystems.

IP Reuse Tools

IP reuse tools let designers package their IP to enable rapid assembly of an entire subsystem or SoC with IP blocks. Integrators can create and begin verification of complex subsystems in a matter of hours, rather than days, greatly reducing overall cycle times. Synopsys offers a complete family of tools for single IP blocks and IP-based subsystems that enable designers and integrators to create and support complex IP faster and more easily.

- coreBuilder for efficient packaging of IP
- coreConsultant to guide the user through core configuration and integration
- coreAssembler for creating and managing packaged IP-based subsystems, including assembly, configuration, and implementation

Synopsys System-Level Solutions

Synopsys system-level solutions offer a combination of tools and system-level IP that enable continuous hardware/software development, integration, and early validation of complete systems. A combination of tools and libraries is used to create complete models of SoCs and devices called the DesignWare Virtual Platform Models (VPMs). Synopsys also provides a comprehensive set of services to aid in the development of these Virtual Platform Models.

Using Virtual Platform Models, developers gain complete visibility and control of the modeled device before hardware is available. This dramatically increases the developers' productivity, resulting in a reduction of time-to-market by 9 to 12 months.

Virtual Platform Models are integrated with the leading software development toolsets, delivering a complete desktop environment for drivers, operating systems, middleware, and application development. Virtual Platform Models execute unmodified production code at near device speed.

Synopsys system-level solutions tools also include Innovator and System Studio. Innovator is a dedicated environment for developing Virtual Platform Models and is complemented by an extensive library of system-level IP. System Studio is used to model SoC behavior and environments. It is also used to analyze and optimize its signal processing algorithms. The extremely fast data-flow simulation is augmented by a large library of signal-processing functions, including specialized libraries for wireless and multimedia standards.

Synopsys system-level solutions tools fully support SystemC™, the leading architecture-level modeling language used to explore complex architectures. It is also integrated with Synopsys' Reference Verification Methodology (RVM) allowing system-level models to be used both as reference models in the ensuing RTL design and verification flow, and as the execution model for embedded software development. This integration ensures that VPMs, architecture models and RTL models remain in sync throughout the development cycle.

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Predictable Success

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