

Design-for-Manufacturing

Synopsys Design-for-Manufacturing (DFM) solutions accelerate time-to-yield through advanced technologies that bridge the areas between design and manufacturing. These technologies span the entire process—from design creation and layout to silicon and yield management. This provides designers with predictable success, improved yield, lower costs, and reduced variability for greater confidence. And Synopsys backs this solution offering with proven results in tapeout and manufacturing, as well as highly qualified and experienced experts to help you throughout the process.

Hercules Physical Verification Suite

The Synopsys Hercules™ Physical Verification Suite (PVS) is the fastest, production-proven physical verification (design rule checking) solution in the market with foundry certified sign-off. Hercules PVS was the first tool to introduce hierarchical processing and multi-CPU technologies to deliver unequalled verification speed (going from 2 days to less than 2 hours). An integrated component of the Galaxy™ Design Platform, Hercules PVS is uniquely positioned to pass information between design and manufacturing. These critical links are necessary to implement and ramp manufacturable, high-yielding processes at the 90 nanometer (nm) process node and below.

- Trusted by leading semiconductor manufacturing companies for accuracy, turnaround, and capacity in their state-of-the-art designs
- Scales across multiple CPUs, over several machines, with best overall turnaround time
- Delivers high productivity with its links to implementation tools such as Star-RCXT™ and IC Compiler

Proteus

The Synopsys mask synthesis solution, Proteus, is a comprehensive, powerful environment for performing full-chip proximity correction, building models for correction, and analyzing proximity effects on IC layout patterns. Its superior programmability and flexibility ensures an optimal match to the designer's objectives and constraints. Proteus is a production-proven solution that has been in production use for 9 years and 5 production nodes. It enhances yield and enables next-generation, ultra-deep submicron designs by modifying layout geometries to improve printability. Key benefits include:

- Flexibility to address optical proximity effects or distortions arising from resist, etch, and underlying topography influences
- Scalable over a large number of processors to provide fast turnaround time at low cost of ownership

PSM Check, PSM Create and SiVL

The Synopsys Phase Shift Mask (PSM) tool suite provides a comprehensive PSM software solution that includes PSM Check and PSM Create. The tools are used to achieve next-generation feature sizes using our strong phase shifting process. The critical layer of the design is split into two masks: a binary mask and a phase-shifted mask. Phase-shifting on gates increases the transistor performance and improves die yield across the wafer through tighter speed binning. PSM Check is used during the design phase to check the layout compliance to PSM process requirements and therefore reduce issues during mask synthesis. PSM Create places and optimizes phase shifters on gate and critical field interconnect to convert existing designs into phase-shifted designs to gain performance and yield.

- Scalable distributed processing reduces the conversion time of PSM designs
- Manufacturing rule check (MRC) and litho-aware placement ensures mask manufacturability
- Production proven to deliver tighter performance distribution

The Synopsys SiVL® (silicon vs. layout) lithography verification tool delivers a fast, accurate way to ensure that the silicon produced with subwavelength geometries will function as intended by the original layout. This innovative IC design-to-manufacturing tool reads in the layout, simulates lithographic process effects, and compares results against the original layout using a high-performance, highly accurate simulation engine.

- Saves time and money by verifying optical proximity correction (OPC) structures based on manufacturing requirements
- Accelerates turnaround time, and lowers mask set costs

CATS

The Synopsys CATS[®] photomask manufacturing data preparation tool has become the de facto standard for photomask manufacturing facilities worldwide. It delivers the most advanced and full-featured data preparation software available for semiconductor photomask manufacturing applications such as inspection, metrology, and direct-write-on-wafer. Plus, CATS offers the scalable distributed processing, enhanced graphics package, proven quality, and mask manufacturing format support these facilities look for to improve their competitive edge.

- Offers hierarchical processing of design data and unequalled compatibility with each machine format
- Minimizes turnaround time while maximizing the quality of high-end masks

Manufacturing Yield Management

Synopsys Manufacturing Yield Management (MYM) solutions accelerate the process customers use to identify, characterize, and eliminate sources of failure throughout the entire product lifecycle.

DSSA Sentry

The large volumes of data within today's fabs, coupled with defect subtleties, make it nearly impossible to find and identify Defect Spatial Signature patterns on semiconductor wafers. DSSA Sentry automatically detects these patterns—in as little as five seconds per wafer—allowing the prevention of potential yield problems or systematic issues before they worsen.

- Fab-proven for many variations of defect signature maps
- Shortens time to detect signature-related yield problems
- Offers a variety of reporting and alarming options (MES, e-mail, custom alarms)

Odyssey

The Synopsys Odyssey product line delivers production-proven defect data management for more than 30 manufacturing sites worldwide. This solution leverages more than a decade of development history to provide real-time lot dispositioning, SPC alarming, and a complete set of defect-analysis tools to help fab engineers resolve both random and systematic yield issues. It's a true 24/7, production-proven solution for meeting the growing demands of today's modern semiconductor fabs.

- Efficient, reliable defect result delivery
- Open, vendor-neutral architecture that supports all inspection, review, and classification tools
- Full range of interactive charting, wafer mapping, and reporting capabilities

Recipe Management and Editing (RME)

One of the biggest challenges facing today's fabs is the use of incorrect recipe usage. In fact, this can cost a fab millions of dollars every year. Synopsys RME delivers a powerful, easy-to-use solution to this challenge. RME is a wafer-fabrication, process-tool-independent solution that enables customers to centrally manage process recipes—significantly reducing scrap while enhancing yield and engineering productivity. It features a universal off-line editing module that uses recipe document object model (RDOM) technology that allows engineers to edit process recipes from anywhere on a corporate intranet without sacrificing security.

- Secure, reliable, and efficient management and editing of recipes off-line
- Recipe parameter history, parameter change notification, and audit trail for trace-back and analysis of recipe problems
- Increased tool time availability
- Allows APC systems to programmatically modify recipes at download time

TestChip Advantage Analysis Software

The TestChip Advantage (TCA) is a sophisticated analysis and data reduction software package that leverages the power of the Synopsys Odyssey industry-standard yield management system. TCA software, paired with Synopsys Diagnostic Chipset intellectual property (IP), provides a wide range solution to characterize the random, systematic, and parametric components of yield loss.

- Allows engineers to quickly extract decision enabling information from the wafer test data
- Automated custom analysis set-up drives high quality of results with fast time to results
- Create custom views of the chip experiments for random, systematic, and parametric yield analysis
- Path to root cause for yield-loss assessment through data-mining and correlation capabilities
- Solution spans across the entire range of yield learning needs throughout the technology node life cycle

SYNOPSYS[®]
Predictable Success

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