SYNOPSYS®

# Synopsys and Sony

verification

**Issues**

- Streamline development of a large family of ASICs for consumer audio/video products
- Reduce time and manpower requirements for hardware/software verification
- Meet very aggressive time-to-market goals with faster, low-cost, reliable products

**Solution**

- Synopsys Professional Services
- Synopsys Chronologic VCS™ Verilog simulator
- Eagle™ hardware/software co-verification tools

**Benefits**

- A four-fold improvement in verification throughput
- A four-to-one reduction in the manpower required for verification
- A reusable verification environment for future products that eliminates need for separate test benches and test programs

## Extensible Verification Solution Cuts Time-To-Market For Advanced Sony Consumer Products

Shaving a month off time-to-market can produce a significant advantage in the furiously competitive consumer electronics market. That's what Sony Semiconductor Business Division accomplished with a new streamlined verification environment, developed in concert with Synopsys Professional Services, for its innovative Virtuoso family of integrated circuits.

**"As complex system-on-a-chip applications grow, we need the ability to answer market challenges on all fronts at the same time, including cost, complexity, features, and time-to-market. Our partnership with Synopsys to develop a flexible verification environment has enhanced our ability to produce complex, high-quality ASICs faster and at lower cost."**

Dr. Taner Ozcelik, Sony SBD, Director of Engineering for Audio/Video Data Products

**Business**
Sony Semiconductor Business Division, a division of Sony Electronics Inc., is a leading manufacturer of integrated circuits and a technology leader in developing solutions for newly-emerging and cutting-edge high-performance markets in multimedia, communications, and workstation cache memory.

# time to

The first chip of the Sony Virtuoso family, an MPEG-2 decoder for digital videodisk (DVD) and digital video broadcast (DVB) applications, was developed in record time. The results were so impressive that Sony Semiconductor Business Division plans to use the extensible verification environment for at least seven more projects.

**On the Leading Edge of Digital Technology**
Sony Semiconductor Business Division (SBD), develops innovative, value-added products for audio/video, communication, and computer applications. SBD consolidates the resource needed to design and deliver a broad selection of integrated circuits (ICs) for Sony and OEM products.

The Sony Virtuoso family of ICs is Sony's next-generation digital architecture for consumer audio/video products. It offers industry-leading digital component integration and sets new price/performance standards for DVD and DVB applications. The first Virtuoso IC on the market is the CXD1930Q, an MPEG-2 video audio decoder with more than a million gates. It integrates more features in a single chip than any contemporary competitive alternative, and offers a unique programmable architecture to meet customer-specific application requirements. This powerful combination makes the CXD1930Q, the premier solution for DVB set-top boxes, DVD players, and personal computers (PCs).

"SBD is moving toward a fully defined system on a chip that integrates a significant amount of software," says Dr. Taner Ozcelik, SBD Director of Engineering for Sony Consumer Audio/Video Data Products. "Our balanced hardware/software approach lets us customize application-specific integrated circuits (ASICs) with software upgrades in a variety of application areas simultaneously. We can upgrade or modify DVD and DVB features simultaneously using the same baseline source code. This reduces both time-to-market and development cost."

At the same time, Sony's system-on-a-chip thrust introduces a whole new level of complexity in design and verification.

**Making the Complexity Manageable**

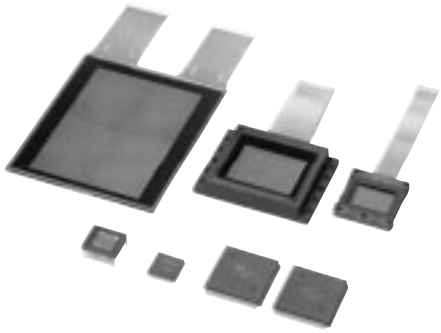
System verification of million+ gate ASICs like the CXD1930Q typically takes up to 40 weeks—too long for SBD's aggressive time-to-market targets for consumer products.

Looking to streamline the process considerably, SBD worked with Synopsys Professional Services to implement a flexible system verification environment for the Virtuoso family. The verification solution had to meet several goals:

- Reduce duplication of effort and risk of error by eliminating multiple environments with separate test benches and test programs
- Eliminate manual checking and increase the execution speed of verification
- Co-verify software and hardware earlier in the process

In addition, the environment had to be easily extensible for reuse on future Virtuoso chip designs.

**In response to the fast pace of digitization in audiovisual equipment, Sony stepped up development and production of key devices to differentiate its products.**



# market

To achieve these goals, SBD teamed with Synopsys Professional Services consultants, recognized for their expertise for developing industry-leading system-on-a-chip process flows and best-in-class verification tools. Key elements of the verification environment are the Synopsys Chronologic VCS Verilog simulator and Eagle hardware/software co-verification tools.

**Best-in-Class Tools for Best-in-Class Products**

Eagle tools enable Sony developers to see the operation of the system hardware and software working together. They can run software with simulated hardware designs at very high speeds to test full-system functionality much earlier in the design process. Software engineers can debug software before the hardware prototype is ready, and hardware developers can verify their designs before expensive prototypes are built. As a result, the delivered product is more likely to be right the first time, saving both development time and money.

SBD selected the Synopsys Chronologic VCS Verilog simulator because of its compliance with all Verilog standards, fast simulation speed, low memory use, and high-level of integration with Eagle. VCS speeds simulation performance by analyzing the coding style and structure of the Verilog design and automatically applying a unique set of optimizations.

**"We did not see any competitive products that could satisfy our needs. Eagle was a perfect tool for what we needed and provided the basic platform. And we were impressed by the high level of synergy between Eagle and VCS."**

Dr. Taner Ozcelik, Sony SBD, Director of Engineering for Audio/Video Data Products

In addition, experts from Synopsys Professional Services assisted in the development Tcl test scripts that SBD can reuse and easily extend with new Tcl commands.

"We did not see any competitive products that could satisfy our needs," Ozcelik says of the Synopsys tools. "Eagle was a perfect tool for what we needed and provided the basic platform. And we were impressed by the high level of synergy between Eagle and VCS."

**It All Comes Down to One Thing–Faster Time-to-Market**

This flexible environment helped SBD design, verify and produce a working prototype of the CDX1930Q in less than six months, a significant achievement for such a complex design. The CDX1930Q introduces very complex, state-of-the-art technology for both DVD and DVB on a single chip. "In a sense, we began with a very complex chip design to open the road beyond it," explains Ozcelik. "Follow-on chips in the Virtuoso family will include capabilities for digital television, digital cable, and wireless cable, as well as DVD and DVB."

SBD had the evaluation board up and running in less than a week, compared to two months for a similar design. The evaluation board used the same software driver code as the Verilog register transfer level (RTL) model of the chip. That means if software changes are required during board evaluation, SBD can port back the same code and run RTL regressions. These features helped reduce the CDX1930Q's time-to-market by more than a month, a huge competitive advantage in the fast-paced semi-conductor marketplace.

"The synchronization between the pre- and post-tape out verification is the most impressive element of the new environment," says Ozcelik. "We were able to use the same inspectors and completely verify the system without changing a single line or character in the code." This saves SBD substantial amount of verification time and is critical in meeting time-to-market goals with new products.

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**Conclusion**

The results of SBD's verification environment speak for themselves. The evaluation board was ready in only a week. Automation allowed one person to do the work of a four-person team. Verification was completed a month faster than usual. Since introducing the CDX1930Q chip, SBD has ported their extensible verification environment for use on another chip design and plans to employ it on at least seven more projects.

"As complex system-on-a-chip applications grow," concludes Dr. Ozcelik, "we need the ability to answer market challenges on all fronts at the same time, including cost, complexity, features, and time-to-market. Our partnership with Synopsys to develop a flexible verification environment has enhanced our ability to produce complex, high-quality ASICs faster and at lower cost."

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