

Synopsys and LANcity

LANcity Adopts Design Reuse with DesignWare® to Bring Low-Cost, High-Speed Cable TV Modem to Consumer Market

What does it take to redesign a commercial product for a highly-competitive consumer market? How can a small company, competing against industry giants, reduce product size, decrease cost, improve their technological edge—and be the first to market?

“DesignWare is critical for a design reuse methodology because it provides a technology-independent core. With DesignWare and a commitment to a design reuse methodology, the vendor selection can be a business decision first and a technology decision second.”

Kurt Baty, Design Consultant

DesignWare

Solutions

- DesignWare IP Library
- Design Compiler™
- HDL Compiler™
- Design Analyzer™

Benefits

- Fastest route to silicon. Increases designer productivity through automatic gate-level
- Proven solution. World's most widely used logic synthesis product family proven in 50,000-plus designs with more than 60 semiconductor vendors
- Promotes high-level design exploration and trade-off analysis through architectural synthesis
- Provides easy menu-driven graphical control of Synopsys' synthesis tools

These were the questions facing the management and design team at LANcity Corporation in their quest to create the first cable TV data modem for the consumer market. Cable TV modems, allow transmission of high-speed data (such as fast Internet and interactive data) through cable TV coaxial systems. LANcity Corporation, a pioneer in cable TV modem

technology in Andover, MA, has been providing bridges and IP routers for cable TV operators, schools, cities and federal government institutions since 1990. The company's first products, however, were designed for industrial use—too large to sit on top of most televisions and too expensive to be competitive in the consumer market.

Speed

To make their technology available to the general consumer, LANcity established three key objectives for their new modem design:

- Integrate the system into a few chips to reduce size and cost
- Improve the performance and manufacturability of their product
- Get it to market long before the competition at highest quality

Combining design reuse with low-power deep submicron technology, LANcity introduced their cable TV modem to the market in less than one

year. The design team started coding at the end of March 1994. The team finished in December, having dedicated 50 percent of the time to functional simulation and taped out in January. The new cable TV modem, unveiled in May 1995 at the National Cable TV Association show in Dallas, TX, offers bi-directional, 10 megabits-per-second performance over 200 miles using existing cable TV. Size, cost, performance, and time-to-market goals were achieved: the cable TV modem, which is 6 inches by 9 inches in size, is about 1,000 times faster and a fraction of the cost of conventional telephone modems.

Short Time-to-Market

In redesigning their first generation cable TV modem, the LANcity team knew they would need to reduce system size for the consumer market. On the previous system, for example, analog circuitry alone took up 80 square inches on one board. The key to successfully reducing size and cost was high integration, including a custom DSP that would integrate much of the existing functionality into a single chip.

But with high integration comes high complexity and more chances for things to go wrong. The design team would have to be sure that their design worked, long before they got to the gate-level. The team turned to high-level design, relying heavily on state-of-the-art simulation and synthesis

tools to identify problems early in the design cycle. (See, "Design Flow at LANcity.")

LANcity's design team, led by vice president of engineering Chris Grobicki, was made up of veteran IC design consultant Kurt Baty and four other engineers. John Ulm designed their first protocol chip and brought considerable digital design experience for architecting the new chip design. Paul Chamberlain was the test programmer who wrote some of the Verilog code. Bill Corley was the analog architect who coded the QPSK modem design and DSP technology, including the analog gain control (AGC) code, one of the most intensely complex aspects of the design. Jerry Lampert was the engineer responsible for the board design and the glue logic.

# of Operations/Second	Operation	Component	Instances
1.66B	x	DW02_mult	72
480M	Σ	DW02_sum	14
660M	+	DW01_add	33
125M	Sin	DW02_sin	5
125M	Cos	DW02_cos	5
20M	÷	DW02_divide	1
20M	Arctg	DW02_arctg_yx	1
20M	$\sqrt{x^2+y^2}$	*	*
975M	Roundings	**	**
Totals: 4.09 Billion	9	7	131

* Specially developed part for LANcity
 ** Added to DesignWare Libraries in a later release

Figure 1: DesignWare Components Used in LanCity DSP ASIC

A Successful Recipe with DesignWare

In early 1991, LANcity had adopted Synopsys development tools and became an avid supporter of the design reuse methodology, including use of the Synopsys DesignWare IP Library, as recommended by Kurt Baty.

For the new cable TV modem design, DesignWare IP Library provided vector adders, multiply, sines, cosines and divide, and Baty developed the root sum of the squares and the arctangent of y/x, as well as synchronous counter blocks from an earlier

LANcity design. The combination of the design reuse code made up more than 50 percent of the final design.

"The design reuse methodology is incredibly efficient," Baty stated. "The vector adders were especially valuable. Using DesignWare we duplicated a section of circuitry from the protocol chip to save going back and forth between a couple of pins. We still had a lot of coding to do, but DesignWare was the recipe for success for us." (See figure 1)

High Integration Turns Up the Heat

LANcity's new chip was a QPSK modem with specific DSP requirements for the cable TV industry, encompassing most modulation and demodulation functions, as well as cable TV aberration gain control and equalization functions. There were multiple advantages for LANcity. By replacing the existing analog circuitry with a component that is inherently cheaper and more reliable, they were saving board area and money. The custom DSP also made the product more robust,

providing dramatically better ability to operate under impaired channel conditions than was possible with the previous generation of the product.

The custom DSP IC performs more than four billion computations per second. With 60 square inches of the original analog circuitry packed into this 155,000-gate ASIC, the entire system now fits on a single 6 inch-by-9 inch PCB.

The team was concerned that the combination of high

performance, high speed and integration would generate more heat than the chip could handle. The designers had to find a way to reduce power or dissipate the heat. After examining the alternatives, the team made the technical decision to use an advanced 3.3-volt, 0.5-micron design strategy. As a 3.3-volt device, the custom DSP would generate significantly less heat. The decision to move to an advanced technology helped solve the heat issue, but made the choice of ASIC vendor even more critical.

Making the Decision for Deep Submicron

One of the strongest advantages provided by DesignWare IP Library was the freedom to make the best business decision in selecting an ASIC vendor.

The arithmetic and register files developed through the design reuse modules amounted to more than 80,000 gates that the design team knew worked. LANcity could compare the heavily used parts of the design to the vendors' cell libraries and determine if the cell libraries would be more efficient than LANcity's modules. Using the

vendor cells, which are optimized for the vendor's technology, reduces the number of gates used as well as the die area.

But vendor libraries became a secondary deciding factor because of DesignWare. LANcity had the choice of using the design reuse modules and moving directly into production, or using the modules as a prototype to model the vendor cells and getting the same or better results. With that knowledge LANcity was free to look at all the possible technologies and make the best business decision.

In the end, AT&T's 0.5-micron, 3-volt process offered the most attractive possibilities, both economically and technologically. The only modules replaced by an AT&T cell were the multipliers.

"We didn't have to choose a particular vendor because they might have the libraries we needed," Grobicki noted. "In fact, the first seven months of design were performed using another vendor's 0.6-micron library. The 0.5-micron AT&T libraries were effortlessly added six weeks before the design was given to AT&T for layout."

According to Gary Gasper, ASIC strategic marketing manager for AT&T Microelectronics, the flexibility of DesignWare and the systems-on-silicon focus of AT&T Microelectronics provide benefits for designers. "DesignWare offers customers the flexibility to quickly evaluate the functionality of their design prior to ASIC vendor selection," Gasper said. "The customer can then make the necessary price/performance trade-offs by retargeting their design to competing ASIC vendor libraries. AT&T's broad ASIC library offering in leading-edge technologies complements DesignWare very well."

Future Plans

"LANcity definitely got its mileage out of DesignWare," Baty concluded. "DesignWare is critical for a design reuse methodology because it provides a technology-independent core. With DesignWare and a commitment to a design reuse methodology, the vendor selection can be a business decision first and a technology decision second."

LANcity's use of DesignWare IP Library components significantly

decreased the design time of the DSP ASIC, resulting in faster time-to-market for the cable TV modem. "For our DSP ASIC, we used DesignWare components for 80,000 of the 155,000 gates," Grobicki noted. "With DesignWare as part of our design reuse strategy, we were able to complete this highly complex design, from start of coding to tape-out, in just ten months. Without DesignWare, it would have been 12 to 16 months of work—time we just couldn't afford." When LANcity respins

the chip to achieve even higher speeds, DesignWare will play a role in the new part.

"At LANcity, we look for the tools that help us design most efficiently," said Grobicki. "Synopsys tools, including Design Compiler synthesis and DesignWare, helped us meet our design goals and create a commercial product that was first to market in its field." (see figure 2)

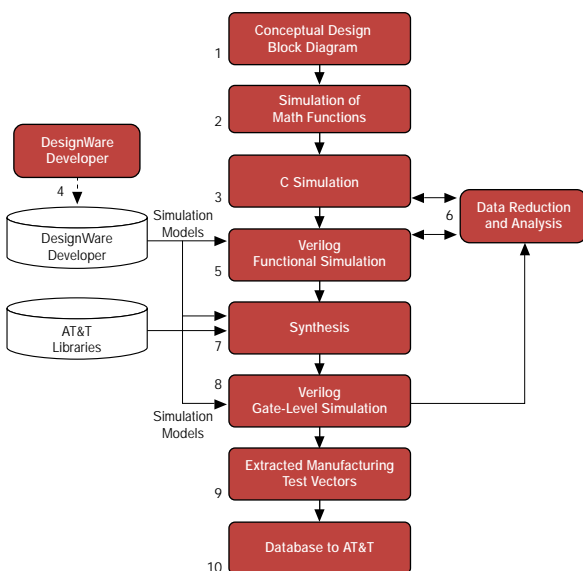


Figure 2: Design Flow at LANcity

1. The design process at LANcity began with the creation of a conceptual design block diagram for the analog portion of the design.
2. Working from the block diagram, the analog designer modeled the math and ran high-level simulations to confirm the design architecture.
3. When the high-level design was validated, the designer began coding the system in C, then simulating to verify their implementations.
4. At the same time, work began on implementing the necessary functions in Verilog. The designers used existing

- functions from the DesignWare IPLibrary as well as new functions written by consultant Kurt Baty using the DesignWare developer tool. The DesignWare functions were combined with additional glue logic to implement the entire DSP ASIC.
5. The designers ran the same test cases in Verilog and in C for an independent check of the algorithm during development. During simulation, the DesignWare functions were modeled using the Verilog simulation models provided with the Foundation Library.

6. The results of the C simulations and the Verilog functional simulations were continually compared, using automated data reduction and analysis tools to verify that the Verilog description delivered the required functionality.
7. LANcity used Synopsys' HDL Compiler to prepare the Verilog description for synthesis, then used Design Compiler to synthesize the design and Design Analyzer to analyze the synthesized output. It was not necessary to have selected an ASIC vendor early in the design process since the DesignWare IP Library was available. Once LANcity had made the selection of AT&T, a cell from the AT&T library was chosen to replace one of the DesignWare components used during synthesis.
8. Post-synthesis, the team performed additional simulation on the gate-level design, then used their data reduction and analysis tool to analyze and compare results with the earlier, higher-level simulations.
9. Their final task was to extract manufacturing test vectors.
10. The design database was ready to hand-off to AT&T.

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