

# Synopsys and Creative Technology

## Creative Technology & Synopsys Team for Design Productivity

### Creative Technology's First Pass Silicon Success

Creative Technology Ltd., a leader in multimedia, has developed a 3D graphics board containing a proprietary ASIC co-developed by Creative Technology and 3Dlabs Inc.

They attribute much of their success to Synopsys' high-level design (HLD) solution. With the help of the VHDL HLD methodology, the team succeeded in meeting their aggressive time-to-market and quality objectives.

**"We were given a very short period of time to learn and implement an unfamiliar HLD methodology. The use of VHDL has been a major advantage, due to its ease of use and reusability. It was especially important in our project when specification modifications had to be implemented rapidly. We are very happy with the results of Synopsys' HLD solution and will incorporate this new design methodology in our future projects."**

Christophe Bouquet and Niranjan, engineers in the Singapore design team

# VHDL

### Solution

- VSS™
- Design Compiler™
- DesignWare®
- SmartModel Library™
- Test Compiler™

### Benefits

- Real-time 3D true texture graphics
- 25 million pixels/sec fill rate
- Accelerates 8-bit and 16-bit 3D rendering
- Accelerates transparency and fogging
- 16-bit hardware z-buffering and double buffering
- On-board z-buffer and texture memory
- Expandable to 4 MB DRAM with daughter memory card
- Works with all popular VGA solutions
- Supports scores of popular DOS and Win95 games

### The Project

Creative Technology has taken the leadership position in providing an affordable 3D graphics solution to the PC market with the introduction of 3D Blaster. The ASIC, code named "Gigi," delivers 3D features and quality comparable to those of high-end workstations, at PC prices.

Gigi is a 304-pin, 180-k-gate ASIC designed entirely in VHDL with the use of Synopsys' HLD solution – synthesis, simulation, and test synthesis.

# synthesis

According to K.K. Ng, the principal engineer in charge of the ASIC project, "The greatest challenges we faced in the project were the pressures to design a highly complex ASIC within a short period of time. The team needed to quickly establish a high-level design approach in order to meet the objectives. Complications also

arose because the project was a coordinated effort among various design teams located in three different countries (Singapore, the USA, and the UK). Great emphasis was placed on the specifications definition and making sure that all the teams strictly followed their respective schedules."

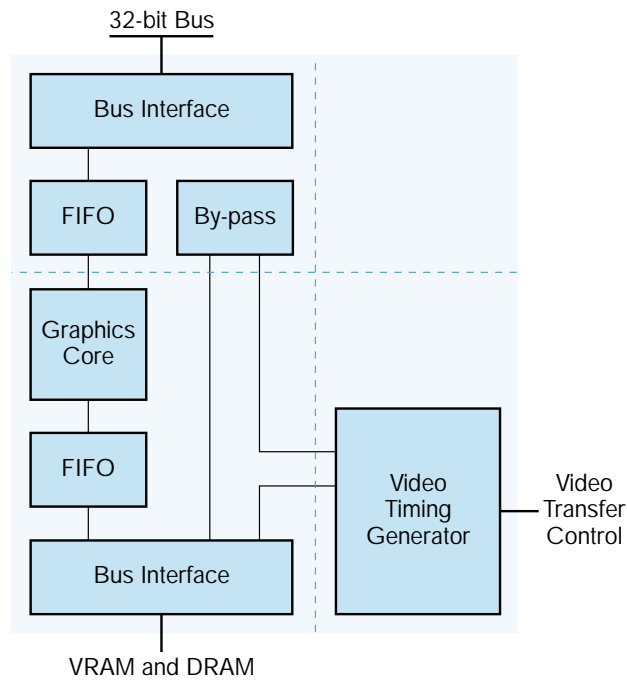


Figure 1: Internal Structure of the ASIC

### Design Architecture

The major part of the ASIC (figure 1) consists of a very large optimized pipeline, making use of multi-stage buffering to reduce the latency and maximize the throughput. The chip can be divided into multiple clock domains with the main graphic core clock running at 40 MHz.

The design is hierarchical, partitioned according to functionality, to maintain clarity and facilitate efficiency in module synthesis and simulation. Most of the modules maintain the same structure and have a single cycle path at 40 MHz. This facilitates reusability between different blocks and enables the use of systematic scripts during the synthesis process. All the modules constrained by a 1 pixel per clock cycle managed to achieve this throughput.

**Simulation Strategies**

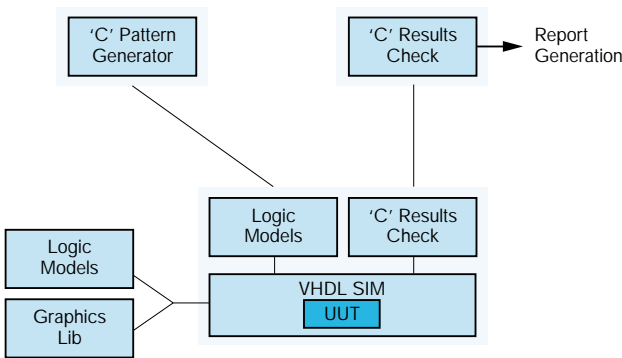
According to Chris, "Simulation was carried out extensively at all stages of the design to ensure full verification of the chip. VSS, with its unique C language interface (CLI) and single kernel for behavioral, RTL, and gate-level simulation helped us to achieve our goals."

The verification strategy for the chip is shown in figure 2.

The low-level signaling protocol testbenches were written in VHDL, while the CLI interface layer allowed importing of stimuli generated by C code. The main advantage of this arrangement is fast debugging of the first silicon. The CLI provides a standard interface to the test, making it possible to reuse exactly the same test format for most of the modules in the design. The CLI also enables gathering of data to a

C graphics library which displays the output of the chip as it would appear on the final system. This feature was very useful and helped the designers to check against possible specification mistakes early in the design cycle.

Emphasis was on RTL simulation rather than gate-level simulation due to the great amount of time that can be saved in verification at the RT level and due to the



**Figure 2: Verification Strategy for the ASIC**

design team's confidence in the synthesis process. All the tests were automated using scripts, and logged to facilitate testing and diagnostic phases.

VSS Expert™, with a single simulation kernel and multiple engines (interpreted, compiled and gate-level) enables the use of a common interface and test patterns at the gate-level simulation phase. During pre-layout simulation, a clock skew using a VHDL generic variable was introduced to emulate possible delays after placement of the clock tree. Validation of

the design was done with both minimum and maximum estimated clock skew. Individual modules were first simulated at the gate level to reduce testing and debugging time. Next, non-redundant necessary tests were run as the different design blocks were assembled. At this stage, we emphasized block interfacing and data flow through. The design team's use of VSS for the final gate-level simulation enabled them to stay in a single VHDL language environment all the way through sign-off simulation with their ASIC foundry. Due to the com-

plexity of the design, gate-level simulation required a minimum of 500 MB of RAM and 1 GB of swap space, on a Sparc 20 platform.

The extensive simulation testing done at the RT level, gate level and board level proved to be very rewarding during the debugging of the first engineering sample of the silicon. The chip was up and running in less than 24 hours. In addition, full-function board verification was completed in less than three days. (Remarkable for a chip of this size and complexity!)

### Synthesis Strategies

"Design Compiler Expert, with its powerful script command, enabled a systematic approach to synthesis that was critical to the success of a design of this size, involving a team of developers.", said Niranjana

A bottom-up approach was employed, with each module being synthesized individually with over-constraints. Over-constraining at the individual module level allows for scan insertion, routing delays, and changes of wireload model during the integration of all the modules to meet the chip's overall timing constraints.

Certain features, such as the use of auto-wireload model, helped reduce the problems of integrating the modules. The commands "load\_of" and "drive\_of" were also used to set correct driving and loading cells for a cell with typical characteristics. Design Compiler was also used extensively for

static timing analysis of the compiled design to speed up timing verification of the design.

According to K.K. Ng, "The use of DesignWare components helped us to meet the timing goal of one critical module in a very short time, rather than redesigning the entire block. This made a significant contribution to reducing the time to market."

### Test Synthesis Strategy

Due to the complexity of the design, it was implemented with the full- multiplexed scan using Synopsys Test Compiler Plus. Chris said, "Full scan was chosen as the safest and most reliable method to achieve high fault coverage for a 180-k-gate design. It is nearly impossible to do it using hand-generated functional tests. The decision to use full scan, although it increased the area of the chip, provided us with high fault coverage coupled with short time to design."

### Conclusions

The Creative Technology design team experienced increased productivity in adopting a high-level design methodology. HLD helped them to meet a demanding schedule, achieve short time to market, and meet quality objectives.

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