

# NanoSim: A Next-Generation Solution for SoC Integration Verification

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The convergence of consumer electronics and personal computing continues to drive the need for more powerful, complex and highly integrated IC design, fabricated with the latest manufacturing technologies. At the same time, the demand to lower cost and power consumption in ICs — plus the ever-shrinking market window — results in more than 50 percent of today's IC designs using system-on-chip (SoC) technology. Needless to say, designing such complex chips is a daunting task.

Equally challenging is the task of ensuring that the chips meet functional, timing and power specifications and work right the first time. According to an independent market study, at 0.13 micron, up to 45 percent of all designs will require at least one additional full mask-set iteration, costing close to \$1 million per set. If you factor in the potential loss due to missing the market window, the cost becomes enormous. To address these many integration challenges, a next-generation SoC verification solution is required to ensure success.

## Traditional Approaches to SoC Verification

Traditionally, different teams verified the digital and analog portions of an SoC design. For instance, the digital design team would follow the top-down design approach, using either Verilog and/or VHDL simulators to verify the design first at the register transfer level (RTL) and then at the gate-level, after logic synthesis. The analog design team, however, would start from the bottom up using a SPICE simulator to verify the design at the transistor level. The teams would verify intellectual property (IP) blocks based on whether they were digital or analog and on the block's design abstraction level (RTL, gate-level, SPICE or Verilog-A netlist). Then, the integration team usually performed the final functional verification of the entire SoC at the very end of the design cycle, after the design had been stitched together. Since it was impossible to verify the entire design at the transistor level with SPICE, a digital approximation of transistor-level blocks was often used to allow the design to be verified using digital simulators.

A main concern with this traditional approach was that integration verification occurred too late in the design cycle to allow for the efficient repair of any integration errors that were discovered. Also, reliance on separate simulators introduced inherent inaccuracies. The deficiencies in this approach often resulted in costly and frequent design re-spins.

## Big D, Little A vs. Big D, Big A Simulation

In the last decade, commercial EDA tools have emerged to enable co-simulation of digital and analog functions using Verilog/VHDL and a SPICE-based simulator. These co-simulation tools were designed to handle "Big D, Little A" types of designs. But these tools have lacked the capacity and performance to handle today's "Big D, Big A" variety of SoCs, which have equally large portions of digital and analog blocks. A next-generation simulator for SoC integration verification is, therefore, required to handle these complex designs.

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## NanoSim: The Next Generation in Big D, Big A Simulation

Synopsys' NanoSim™, integrated with VCS™, is a prime example of this next generation in Big D, Big A simulation. It delivers a single-kernel solution for high-performance Verilog/VHDL simulation that can be readily adopted into any transistor-level verification flow to address multi-level mixed-signal verification needs (see Figure 1).

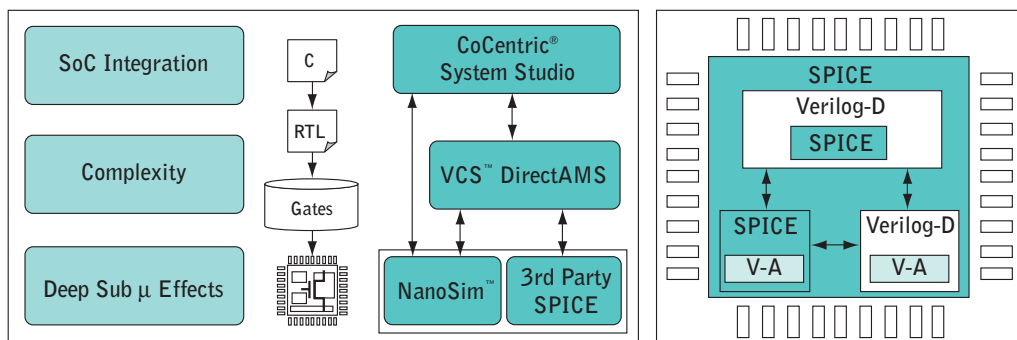


Figure 1. NanoSim – Full-chip MLMS solution for SoC integration verification.

NanoSim supports design abstractions in RTL, gate, and SPICE — so integration verification can be performed at all phases of the design cycle. It also supports analog behavioral modeling — such as Verilog-A and C models — so that a top-down, analog verification method can be deployed. One key benefit is the ability to verify the entire system at the specification level to allow better architecture and IP selection. In addition, NanoSim offers the flexibility to handle the verification of a variety of embedded IP, such as a Verilog-based IP with a SPICE netlist or vice versa. Last but not least, NanoSim supports multi-level, mixed-signal verification of “Big D, Big A” SoCs, such as high-performance designs with built-in Phased-Lock Loop (PLL) circuits.

With the most extensive support for SPICE netlist formats available on the market today, NanoSim is easy to adopt into any transistor-level verification flow and addresses multi-level mixed-signal verification needs. It is easy to use, offering an intuitive GUI and automatic insertion of a digital/analog interface that is transparent to users.

## Conclusion

As process technology continues to advance below 100 nanometers, the cost of leading-edge SoC design plus time-to-volume pressure will no doubt continue to rise. To ensure that designs work right the first time, a next-generation simulator for SoC integration verification is required. This simulator must be able to handle very large digital and very large analog blocks effectively, and to simultaneously simulate a wide variety of design abstractions from RTL, gate, transistor and analog behavioral models. Companies that deploy the right solution will be in the best position to benefit from improved competitiveness and profitability.

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