Datasheet

SYNOPSYS®

MVRC

Static Voltage-Aware Verification

Overview

Power management has become a critical issue due to the proliferation of handheld and wireless devices and the incessant march to smaller geometries. Power-management techniques range from the usage of clock-gating and multi-threshold libraries to voltage-control techniques such as power gating, retention, dynamic voltage scaling (DVS), and low-vdd standby. Designs employing voltage control techniques pose an ever increasing verification challenge. The verification complexity grows with the number of distinct power states in a design. A design needs to be verified as it progresses from the RTL stage to netlist. At each stage in the design, the power management implementation must be checked for compliance with the power intent. A single error could place the design in an unknown state causing the chip to malfunction. True voltage-aware static checkers for power management verification must be aware of multiple-voltages and their interdependencies. MVRC is a voltage-aware static checker that allows engineers to rapidly verify the designs that use voltage control techniques for power management. Additionally MVRC enables verification of the correct implementation of protection circuitry from an architectural and structural perspective.

MVRC Key Features and Benefits

- Rapidly finds power management bugs without the need for test benches, thereby speeding up design verification time
- Validates the power architecture of the design
  - Validates integrity of control signal networks across voltage islands
  - Derives safe power sequences
  - Performs structural checks based on power intent
    - Detects bugs in the logic and power connection of protection cells
  - Automatically derives the power state table for designs with hierarchical power management
    - Eliminates months of power intent specification time
  - Set-up time is minimal; easy to install and use for design verification
  - Customizable error and warning messages allow for easy integration with customer's flow

MVRC validates power intent across the design flow

MVRC takes in RTL or gate-level netlist representation of the design in either Verilog or VHDL. It reads the .lib file for definition of protection cells. It accepts the power intent specified in industry standard Unified Power Format (UPF).

MVRC can be used to check the design for functional checks after the RTL has been frozen, or for Netlist hand-off after synthesis. MVRC can also check the implementation after Place and Route. It outputs a log file and an error and warnings report for all violations related to multi-voltage checks. See figure 1.

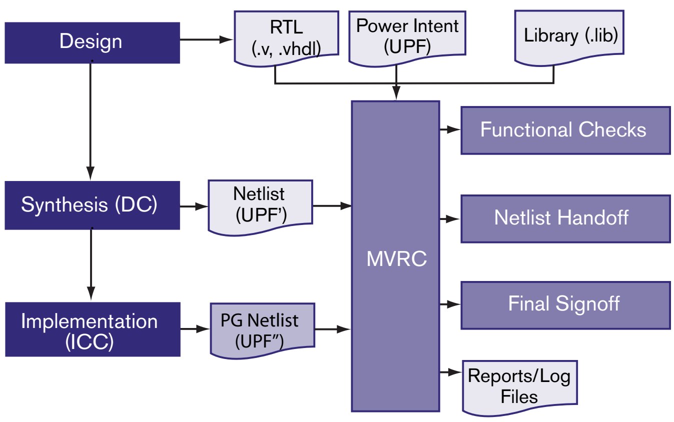

Figure 1: MVRC validates power intent across the design flow.

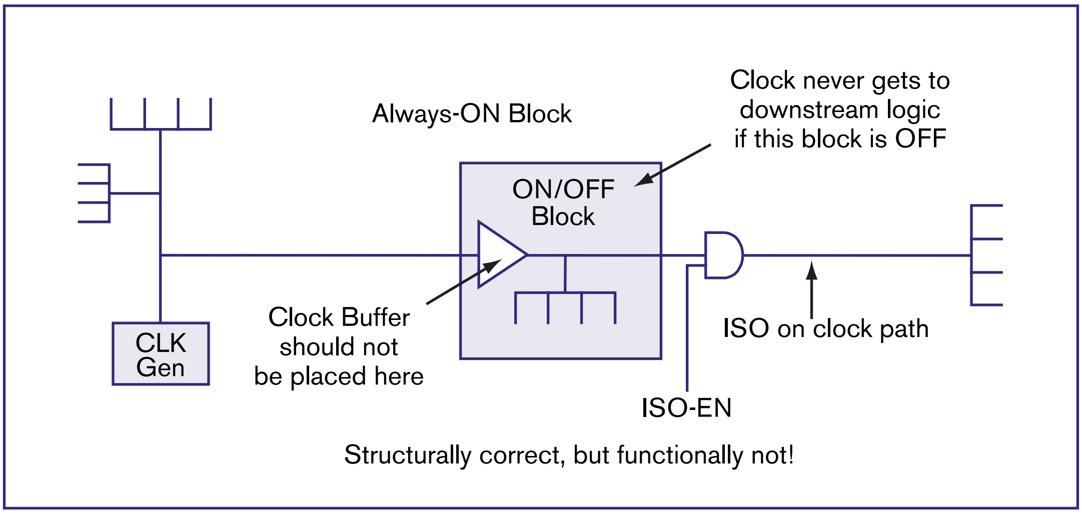

Figure 2: MVRC detects structurally correct but functionally incorrect clock-tree implementation.

Unique Value of MVRC

- In addition to the structural checks on the isolation and level shifter cells in the design, MVRC has the unique capability of performing architectural checks. MVRC validates the design in its entirety and checks the critical signal networks in the design (clock, reset, power-enable, isolation-enable, scan signals etc.) for the various power modes. These checks help find connectivity related bugs which would cause functional issues for the regions that are powered up in a design
- MVRC understands the power intent of the design and performs an analysis of the power state table as defined in the power intent. MVRC checks all intermediate power-states and reports unsafe states that are likely to cause power management issues
- MVRC checks the power-state table for violations of the power specification. It derives a correct sequence for power-up and power-down modes based on the power intent
- Designs with a large number of voltage islands benefit from the automatic derivation of a hierarchical power-state table. MVRC understands the power intent and is able to prune a large number of power states to a few distinct ones, thus reducing the effort involved to specify and then verify all the power management functions

Example

Figure 2 shows an example of bug that MVRC excels at detecting. In this example, a clock buffer has been incorrectly placed in an on/off voltage island. An on/off voltage island can be turned off and will be unable to drive the downstream clock signal in an always-on block. The clock buffer is structurally correctly placed and a verification solution that only checks for correct placement of an isolation cell will fail to detect that this is an error. MVRC's micro-architectural analysis algorithms have complete understanding of the power intent of the chip. MVRC is also truly voltage-aware and comprehends that this placement is illegal and will likely cause a functional failure. It will report the situation as an error.

Conclusion

Power management techniques are increasingly used to combat leakage and dynamic power consumption. Multi-voltage designs require comprehensive verification coverage of all voltage-control techniques. MVRC is a truly voltage-aware static verification solution that understands the power intent and rapidly checks for power management design violations. MVRC is production proven in many customer designs.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

Synopsys® Predictable Success

Synopsys, Inc.
700 East Middlefield Road
Mountain View, CA 94043
www.synopsys.com