

CHIPit Platinum Edition

Part of the Confirma™ ASIC, ASSP, SoC Verification Platform



Overview

The CHIPit Rapid Prototyping Plus platforms provide functional verification and validation throughout the entire SoC and ASIC design and verification process. CHIPit platforms give design engineers superior speed and flexibility for hardware verification, pre-silicon software development, and system validation. The multifunctional system can be used in multiple verification modes, including cycle/event – based co-simulation, SCE-MI compliant transaction-based verification and in-circuit prototyping to significantly reduce the overall design and verification time. The patented programmable interconnect architecture in combination with a comprehensive software suite enable more automation and the highest productivity for design implementation, verification and debug.

CHIPit Use Modes

Through the support of various verification modes, the CHIPit system provides hardware verification and pre-silicon software development in one single solution.

Hardware assisted verification acceleration

CHIPit enables the efficient debug and verification of designs by reducing turnaround times through its automated, incremental and parallel design implementation flow and by using its integrated debugging capabilities to provide in-depth visibility into the design. The seamless integration of the VCS HDL simulator via the CHIPit HDL-Bridge offers a smart out-of-the-box solution for co-simulation. In addition, CHIPit enables the user to significantly accelerate co-verification by using CHIPit's Transaction Based Verification Modes which deliver up to 10,000 times the performance of pure software simulation. Using the In-Circuit Prototyping Mode hardware design engineers can run extensive and verbose in-system simulation tests to reach deep corner cases and hard-to-find bugs. The flexible, standardized extension board concept allows the user to integrate real-world peripherals at close-to-real speed into the test concept.

Pre-silicon software development

CHIPit is the ideal solution for pre-silicon software development by giving software developers access to a prototype at the earliest possible time in the design cycle. Different versions and subsystems of the design can quickly and easily be loaded into the CHIPit system via CF card, Ethernet or the UMRBus Communication System. After connecting the embedded software debugger to the JTAG interface the user can immediately begin to validate and test the software or firmware at high speeds using their known software debugging environment and IDE.

System Features

Innovative system architecture

The CHIPit Platinum Edition is built on an innovative system architecture concept using the latest FPGA technology and largest capacity. The system is scalable up to 18 FPGAs and handles design capacities up to 36 million ASIC gates. This system can be scaled in increments of 6 million ASIC gates simply by adding additional FPGA boards. The system also provides on-board SSRAM memory modules that can be accessed directly from the FPGAs and can be easily pre-loaded and read back from the host system.

Highest flexibility with 3D Switching Technology

The patented “3D Switching Technology” uses a programmable structure of high-speed interconnects between all FPGAs and extension boards present in the system. These interconnects allow architectural trade-offs between different design structures, allowing the user to meet all architectural and performance challenges. The connection topology is automatically created and adapted by the CHIPit Switch Routing software.

Open system architecture

The CHIPit Platinum’s open system architecture concept offers three extension board sites with a total of 1920 free user I/Os. The use of extension boards allow implementation of high speed interfaces to the user design, like PCI Express, DVI or USB 2.0 and are used to connect to the real world environment.

Easy design implementation

The CHIPit solution offers a comprehensive set of software tools for a guided, automated and easy-to-use design implementation flow. The fully TCL scriptable software guides the user through the flow step by step, offering only options relevant for a specific implementation step. The support of parallel and incremental design synthesis guarantees short bring up and turnaround times and helps to further reduce the implementation time for repetitive design changes.

Powerful communication system

The UMRBus Communication System is an easy-to-use, out-of-the-box communication interface to interact with the CHIPit system for data transfers, monitoring and debugging. It can be used for various applications like memory pre load and read-back, data streaming, bus monitoring or on-the-fly modification of signal values. It is also used internally for platform configuration and management.

Extensive debug capabilities

Various debugging tools are included in the software suite to enable designers to easily find bugs hidden deep in complex designs at high speed.

Verification Modes

Co-simulation mode

HDL-Bridge is a powerful tool that provides a direct link between selected system parts running in the RTL simulator and parts running in the CHIPit system. This allows, for example, to move the DUT of a verification

environment into the hardware for acceleration while still keeping the (unsynthesizable) test bench in the simulator, or to run a stable part of the SoC in hardware while still keeping the rest in the simulator for higher debug visibility. The CHIPit co-simulation interface works with all popular RTL simulators like VCS™, NC-SIM™, and ModelSim™.

Transaction-based mode

The CHIPit Transaction Based Environment, enables users to stimulate the Design Under Test (DUT) from the host side by a C/C++, SystemC or (System)Verilog based testbench on transaction level instead of signal level. This mechanism accelerates the verification dramatically, because the number of data exchanges between host and hardware are minimized and delivers up to 10,000 times the performance of software simulation. The CHIPit transaction-based interface is based on Accellera’s Standard Co-Emulation Modeling Interface (SCE-MI) and supports version 1.1 and 2.0.

In-circuit prototyping mode

In this mode the design runs freely at the highest possible speed in the CHIPit system, allowing testing of the design in a “real world” environment. The mode is mainly used for long and extensive tests or for pre-silicon software and firmware development.

CHIPit Platinum Edition features	
Capacity	<ul style="list-style-type: none"> • Scalable up to 36 million ASIC gates • Scalable: 3, 6, 9, 12, 15, or 18 FPGAs
FPGA type	<ul style="list-style-type: none"> • Xilinx Virtex XC5VLX330
Memory	<ul style="list-style-type: none"> • 3, 6, 9, 12, 15, or 18 x 8 MB SSRAM (depending on number of FPGAs) • SSRAM, SDRAM, DDR, DDR2 available via extension boards
I/O resources	<ul style="list-style-type: none"> • Up to 1920 user I/O pins, on 3 full-size extension board sections • 192 + 6 (regular signals + clocks) connection ports to logic analyzer
Supported design interfaces	<ul style="list-style-type: none"> • Mini-PCI, PCI-Express, USB, DVI, (GBit-)Ethernet, JTAG, RS232, and others (plugged into extension board sites)
Routing	<ul style="list-style-type: none"> • Flexible routable and fixed interconnections
Clocking schemes	<ul style="list-style-type: none"> • Low-skew local and global clock domains • Built-in clock generators • Support for external clocks
Interfaces	<ul style="list-style-type: none"> • Xilinx JTAG interface for all FPGAs • C/C++, Tcl/Tk programming (optional) • Cycle/event based Co-simulation (HDL-Bridge) (optional) • Transaction-based Co-simulation (SCE-MI 1.1, 2.0) (optional)
Configuration interfaces	<ul style="list-style-type: none"> • LVDS (528 MBit/s) UMRBus Communication System • CF card • Ethernet
Others	<ul style="list-style-type: none"> • Stand-alone (bootable system) with integrated self-test • LCD monitoring and control panel
Power	<ul style="list-style-type: none"> • Dedicated external power supply with input 100–240V and 12V output
Dimensions	<ul style="list-style-type: none"> • (498 mm x 281 mm x 278 mm), 20 kg

