

CHIPit Software Suites

Part of the Confirma™ ASIC, ASSP, SoC Verification Platform

Overview

The CHIPit Rapid Prototyping Plus platforms provide functional verification and validation throughout the entire SoC and ASIC design and verification process. CHIPit platforms give design engineers superior speed and flexibility for hardware verification, pre-silicon software development, and system validation. The multifunctional system can be used in multiple verification modes, including cycle/event - based co-simulation, SCE-MI compliant transaction-based verification and in-circuit prototyping to significantly reduce the overall design and verification time. The patented programmable interconnect architecture in combination with a comprehensive software suite enable more automation and the highest productivity for design implementation, verification and debug.

The CHIPit Software

The CHIPit software suites are a comprehensive set of tools for a quick and automated design implementation, powerful debugging and extensive design and software verification. The easy-to-use software guides the user step-by-step through the flow and reduces the time for repetitive design implementation significantly. The various debugging tools provide designers with high visibility into complex FPGA and FPGA-based ASIC prototypes enabling them to find bugs at highest speed. The software also enables the user to link the prototypes to high-level design and simulation environment through the UMRBus or the SCE-MI interfaces to run and verify their designs in verification and validation modes. Depending on his requirements, the user can choose between the following different CHIPit software suites:

CHIPit Manager Base

The CHIPit Manager Base software suite offers various basic features for the project handling, system configuration and monitoring, FPGA interconnection handling and design implementation and contains the following software tools:

CHIPit Configuration Tool

The CHIPit Configuration Tool is for the easy and convenient configuration and monitoring like global clock & reset administration or configuration of the FPGAs, of the CHIPit prototyping systems.

CHIPit Switch Routing

The CHIPit Switch Routing Tool, handles automatically the interconnection structure between all FPGAs of a multi FPGA CHIPit hardware. The tool, which actually comprises a whole suite of GUI and command line tools is used to determine a configuration of the CHIPit system based on a design description. The design description contains all requirements posed by the user with regard to a design which should be implemented onto the CHIPit system.

CHIPit Manager Pro



CHIPit Manager Pro GUI

The CHIPit Manager Pro is the global graphical user interface (GUI) and fully scriptable tool for project management, design analysis and design implementation. It is the cockpit for the complete design implementation flow that handles all required tasks from importing RTL files till in-circuit operation and offers a comprehensive dependency management system enabling an incremental flow for quick iterations. It includes a complete design implementation flow that handles all required tasks from importing RTL files till in-circuit operation. All necessary steps can be done in parallel in order to reduce the design implementation time to a minimum.

CHIPit Manager Pro RTL Compiler

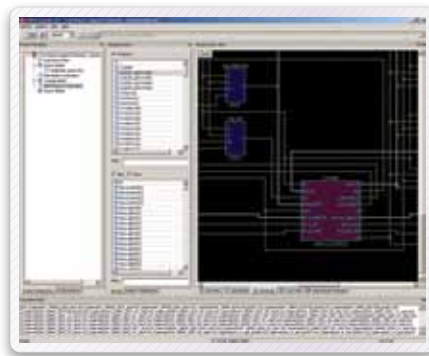
The CHIPit Manager Pro RTL Compiler is an integrated synthesis management and control tool providing an automated interface to Synplify Premier. It allows the user to parallelize the RTL synthesis process on block level in order to reduce the synthesis time dramatically. The software supports the conversion of selected names (hierarchical signal assignments) which allows the user to access internal signals without touching the actual DUT. Furthermore the tool supports the compilation of memory models in RTL into physical memory. The RTL Compiler allows easy black box handling and can even insert a SCE-MI infrastructure for transaction based verification.

CHIPit Manager Plus

In addition to the CHIPit Manager Base suite, the CHIPit Manager Plus software suite contains advanced tools for the design analysis, fast and incremental design implementation including automated design partitioning and extensive debugging. It contains in addition to the CHIPit Manager Base software suite the following software tools:

CHIPit Manager Pro Netlist Compiler

The CHIPit Manager Pro Netlist Compiler performs an extensive design analysis, providing information about clock nets, high fanout nets and black boxes in a hyperlinked design browser with a powerful search engine. The software is linked with the integrated CHIPit Manager Pro Schematic Viewer, which provides the user with unprecedented opportunities to get to know and understand the design. The CHIPit Manager Pro Netlist Compiler includes also a fully scriptable partitioning tool, which is optimized for an easy and more automated design partitioning. The partitioning can be done fully automatically by the tool, manually, or guided by the user.



CHIPit Manager Pro Schematic Viewer

The CHIPit Manager Pro Schematic Viewer is a graphical EDIF netlist analyzer with a design hierarchy browser that provides easy navigation through the design hierarchy and gives a compact hierarchy overview. Furthermore the tool automatically extracts logic cones from user-defined reference points and shows only the relevant portion of the circuit.

CHIPit Debug Suite

CHIPit Visibility Tool

The CHIPit Visibility Tool is a powerful real-time debugging tool supporting multi FPGAs, where all internal FPGA signals can be made visible after place and route. With the tool you can select and route internal signals to debug connector pins without any modification of the design. These signals are available for further tests with a logic analyzer. The Visibility Tool contains a project management module which allows to handle multiple debug versions of a design. For the easy integration of a logic analyzer the software can program a logic analyzer automatically.

CHIPit Host Controlled Debug

The CHIPit Host Controlled Debug software allows the user access to all design registers without any new synthesis and place & route. The signal values are stored in VCD files and can be visualized in a wave form viewer. In the HCD mode the host takes control over the clocks of the implemented design, the software side can suspend these clocks and thus “freeze” the design operation for a certain time span, then let it resume e.g. for another clock cycle and so on, thus effectively single-stepping the design or letting it just run for a certain number of clock cycles. In addition to this, the tool offers the capability to take a snapshot of all selected internal FPGA registers during running freely in the CHIPit system. The values are stored in VCD files and can be visualized in a wave form viewer.

CHIPit Manager Ultra

In addition to the CHIPit Manager Plus suite, the CHIPit Manager Ultra software suite contains entire features for co-simulation purpose and transaction based verification supporting the SCE-MI 1.1 and 2.0 standard interfaces. It contains in addition to the CHIPit Manager Plus software suite the following software tools:

CHIPit Co-Simulation Environment

The HDL-Bridge is a powerful tool that provides a direct link between simulation environment (RTL simulator) and the Design Under Test (DUT) (or a part of it) in the CHIPit system. This allows to run the entire design or parts of it in the hardware during the simulation phase.

Therefore the simulation performance can be improved by moving stable RTL blocks into the prototyping system. Combined with the Signal Tracker for visualizing the internal signals in the simulator, CHIPit provides the user an ideal solution for rapid design debugging. The co-simulation interface works with all popular RTL simulators like VCS™, NC-SIM™, and ModelSim™.

Transaction-Based Verification Environment

The CHIPit Transaction-Based Verification Environment supporting the SCE-MI 1.1 and 2.0 standard interfaces offers the capability to run

the CHIPit system in transaction based verification mode. It helps to accelerate the verification by stimulating the Design Under Test (DUT), from the host side by a C/C++ or System C test-bench on transaction level instead of signal level (minimizing the number of data exchanges between host and hardware). The CHIPit Transaction-Based Verification Environment is seamlessly integrated into CHIPit software environment and provides an ease to use implementation flow.



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