

# CHIPit Iridium Edition

Part of the Confirma™ ASIC, ASSP, SoC Verification Platform



## Overview

*The CHIPit Rapid Prototyping Plus platforms provide functional verification and validation throughout the entire SoC and ASIC design and verification process. CHIPit platforms give design engineers superior speed and flexibility for hardware verification, pre-silicon software development, and system validation. The multifunctional system can be used in multiple verification modes, including cycle/event – based co-simulation, SCE-MI compliant transaction-based verification and in-circuit prototyping to significantly reduce the overall design and verification time. The patented programmable interconnect architecture in combination with a comprehensive software suite enable more automation and the highest productivity for design implementation, verification and debug.*

## CHIPit Use Modes

Through the support of various verification modes, the CHIPit system provides hardware verification and pre-silicon software development in one single solution.

### **Hardware-assisted verification acceleration**

CHIPit enables the efficient debug and verification of designs by reducing turnaround times through its automated, incremental and parallel design implementation flow and by using its integrated debugging capabilities to provide in-depth visibility into the design. The seamless integration of the VCS HDL simulator via the CHIPit HDL-Bridge offers a smart out-of-the-box solution for co-simulation. In addition, CHIPit enables the user to significantly accelerate co-verification by using CHIPit's Transaction Based Verification Modes which deliver up to 10,000 times the performance of pure software simulation. Using the In-Circuit Prototyping Mode hardware design engineers can run extensive and verbose in-system simulation tests to reach deep corner cases and hard-to-find bugs. The flexible, standardized extension board concept allows the user to integrate real-world peripherals at close-to-real speed into the test concept.

### **Pre-silicon software development**

CHIPit is the ideal solution for pre-silicon software development by giving software developers access to a prototype at the earliest possible time in the design cycle. Different versions and subsystems of the design can quickly and easily be loaded into the CHIPit system via SD-Card, Ethernet or the UMRBus Communication System. After connecting the embedded software debugger to the JTAG interface the user can immediately begin to validate and test the software or firmware at high speeds using their known software debugging environment and IDE.

## System Features

### ***Innovative system architecture***

The CHIPit Iridium Edition is built on an innovative system architecture concept using the latest FPGA technology and largest capacity. It is available as a 2 or 4 FPGA version and handles design capacities up to 8 million ASIC gates. The system also provides per FPGA, 8 MByte (2M × 32) SSRAM on-board memory modules and up to 4 SO-DIMM slots for DDR2 and DDR memories, for fast and easy memory access.

### ***Highest flexibility with 3D Switching Technology***

The patented “3D Switching Technology” uses a programmable structure of high-speed interconnects between all FPGAs and extension boards present in the system. These interconnects allow architectural trade-offs between different design structures, allowing the user to meet all architectural and performance challenges. The connection topology is automatically created and adapted by the CHIPit Switch Routing software.

### ***Open system architecture***

The CHIPit Iridium’s open system architecture concept offers up to eight extension board sites with a total of 2560 free user I/Os. The use of extension boards allow implementation of high speed interfaces to the user design, like PCI Express, DVI or USB 2.0 and are used to connect to the real world environment.

### ***Easy design implementation***

The CHIPit solution offers a comprehensive set of software tools for a guided, automated and easy-to-use design implementation flow. The fully TCL scriptable software guides the user through the flow step by step, offering only options relevant for a specific implementation step. The support of parallel and incremental design synthesis guarantees short bring up and turnaround times and helps to further reduce the implementation time for repetitive design changes.

### ***Powerful communication system***

The UMRBus Communication System is an easy-to-use, out-of-the-box communication interface to interact with the CHIPit system for data transfers, monitoring and debugging. It can be used for various applications like memory pre load and read-back, data streaming, bus monitoring or on-the-fly modification of signal values. It is also used internally for platform configuration and management.

### ***Extensive debug capabilities***

Various debugging tools are included in the software suite to enable designers to easily find bugs hidden deep in complex designs at high speed.

## Verification Modes

### ***Co-simulation mode***

HDL-Bridge is a powerful tool that provides a direct link between selected system parts running in the RTL simulator and parts running in the CHIPit system. This allows, for example, to move the DUT of a verification

environment into the hardware for acceleration while still keeping the (unsynthesizable) test bench in the simulator, or to run a stable part of the SoC in hardware while still keeping the rest in the simulator for higher debug visibility. The CHIPit co-simulation interface works with all popular RTL simulators like VCS™, NC-SIM™, and ModelSim™.

### ***Transaction-based mode***

The CHIPit Transaction Based Environment, enables users to stimulate the Design Under Test (DUT) from the host side by a C/C++, SystemC or (System)Verilog based testbench on transaction level instead of signal level. This mechanism accelerates the verification dramatically, because the number of data exchanges between host and hardware are minimized and delivers up to 10,000 times the performance of software simulation. The CHIPit transaction-based interface is based on Accellera’s Standard Co-Emulation Modeling Interface (SCE-MI) and supports version 1.1 and 2.0.

### ***In-circuit prototyping mode***

In this mode the design runs freely at the highest possible speed in the CHIPit system, allowing testing of the design in a “real world” environment. The mode is mainly used for long and extensive tests or for pre-silicon software and firmware development.

CHIPit Iridium Edition features	
Capacity	<ul style="list-style-type: none"> <li>• Scalable up to 8 million ASIC gates</li> <li>• Scalable: 2 to 4 FPGA</li> </ul>
FPGA type	<ul style="list-style-type: none"> <li>• Xilinx Virtex XC5VLX330</li> </ul>
Memory	<ul style="list-style-type: none"> <li>• Scalable 2 or 4 x 8 MB SSRAM (depending on number of FPGAs)</li> <li>• DDR2 and DDR over SO-DIMM (2 FPGA Iridium Edition)</li> <li>• 2x DDR2 and 2 x DDR over SO-DIMM (4 FPGA Iridium Edition)</li> </ul>
I/O resources	<ul style="list-style-type: none"> <li>• Up to 1280 user I/O on 4 extension board sites (2 FPGA Iridium Edition)</li> <li>• Up to 2560 user I/O on 8 extension board sites (4 FPGA Iridium Edition)</li> </ul>
Supported design interfaces	<ul style="list-style-type: none"> <li>• Mini-PCI, PCI-Express, USB, DVI, (Gbit-)ethernet, JTAG, RS232, and others (plugged into extension board sites)</li> </ul>
Routing	<ul style="list-style-type: none"> <li>• 640 switchable interconnections per FPGA</li> <li>• Up to 258 direct interconnections between the two FPGAs on one board</li> <li>• 66 switchable interconnections to SSRAM memory modules</li> </ul>
Clocking schemes	<ul style="list-style-type: none"> <li>• 6 programmable primary clocks</li> <li>• 4 additional primary clock inputs</li> <li>• 7 system-wide clock domains</li> <li>• Clocks can also be driven by User FPGAs</li> <li>• Global reset net, controlled from the menu control panel or by software</li> </ul>
Interfaces	<ul style="list-style-type: none"> <li>• Xilinx JTAG interface for all FPGAs</li> <li>• C/C++, Tcl/Tk programming</li> <li>• Cycle/event based Co-simulation (HDL-Bridge) (optional)</li> <li>• Transaction-based Co-simulation (SCE-MI 1.1, 2.0) (optional)</li> </ul>
Configuration interfaces	<ul style="list-style-type: none"> <li>• SD card, ethernet</li> <li>• LVDS (528 MBit/s) UMRBus Communication System</li> </ul>
Others	<ul style="list-style-type: none"> <li>• Stand-alone (bootable) system; integrated system self-test</li> </ul>
Power	<ul style="list-style-type: none"> <li>• Dedicated external power supply with input 100–240V and 12 V output</li> </ul>
Dimensions	<ul style="list-style-type: none"> <li>• (170 mm × 310 mm × 310 mm), 5,9 kg</li> </ul>