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Predictable Success

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Francesco Sforza
Dynamic Verification Manager
Central R&D,
STMicroelectronics



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Success with the Synopsys® Synplicity® Business Group and STMicroelectronics

Certify® Success Story

Summary

STMicroelectronics has taped out a project that maps automatically generated code onto FPGAs using the Certify® solution from Synopsys' Synplicity Business Group. ST's Dynamic Verification Team demonstrated that in principal the design can move from a high level language all the way to the gate level with no human intervention — with great savings in time-to-market and engineering labor.

ST found the Certify product to be the only tool on the market that provides the FPGA synthesis capabilities needed in this flow. Because of its unique combination of important features, and because Synplicity provides quality support to match, the group has made the Certify solution its standard.

Certify Prototyping Solution Combines Partitioning, Ease of Use, and Quality of Results

STMicroelectronics is a global independent semiconductor company and a leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. An unrivaled combination of silicon and system expertise, manufacturing strength, Intellectual Property (IP) portfolio and strategic partners positions the company at the forefront of System-on-Chip (SoC) technology. Its products play a key role in enabling today's convergence trends.

The Dynamic Verification Team (DVT) within the Central R&D group at ST has a goal of implementing technologies that enable fast prototyping. This activity required an FPGA synthesis solution that is easy to use, produces high quality results, and can synthesize designs that are too large for one FPGA. After evaluating the alternatives, the DVT chose the Certify solution. “As designs grow bigger and bigger, it becomes more and more important, if not vital, to partition them across several FPGAs and perhaps even different families,” said Francesco Sforza, Dynamic Verification Manager for ST Central R&D. “We tried several combinations of products and found that the Certify tool is not only the easiest to use but often produces the best results.”

Automatic Code Generation Project Shows Potential to Save Greatly on Time and Costs

One of the DVT's first projects using the Certify product was to map automatically generated code to FPGAs. The team performed this project for a division of ST that is exploring ways to speed turnaround of new derivatives. “This is a very exciting project because of its potential to greatly reduce time-to-market and engineering labor through automa-

Certify Success Story

tion,” said Mr. Sforza. “Our goal was to implement a streamlined flow that can start with high abstraction level models and go all the way to the gate level without human intervention, including a hardware prototype that can be connected in-circuit to our customer’s certified compliance test suite.”

The flow for this project begins with a design environment that turns a C-like language specification into a golden reference model that can be validated and automatically implemented with verification built into the process. RTL code is automatically generated by this environment and then mapped by Certify software to Xilinx Virtex 2000 FPGAs at the gate level.

The Certify Product — The Only Tool Up to the Task

The DVT tried several FPGA synthesis tools and found that only the Certify product fulfilled the needs of the project. “The other tools had a hard time. The design breaks them,” said Mr. Sforza. “Moreover, the Certify tool includes in a single environment features like Verilog-VHDL mixed language, partitioning, clock-gating handling, and a fast synthesis engine. Even if you can find some of these features in other tools, they are not available in a single environment. Therefore to achieve the goals the user must intervene manually to customize the flow, which is error-prone.”

In October of 2003 the group successfully taped out the design. Although some minor manual fine-tuning was required this time, ST demonstrated that in principal the entire process can be conducted automatically.

The automatic code generation project is just one of the designs at ST that has benefited from the Certify tool. The DVT has other fast prototyping projects in the plan that will take advantage of the Certify product’s ability to handle designs that are too large for one FPGA.

The support that Synplicity has provided to ST matches the quality of its products, according to Mr. Sforza. “Whenever we needed their support, Synplicity quickly provided patches that fixed our problems,” he said.

“This industry is very dynamic and Synplicity’s competitors are all trying to catch up,” concluded Mr. Sforza. “But right now the Certify tool definitely has an edge. That’s why we have chosen to standardize on the Certify prototyping solution.”

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