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Rolf Singer
Mobile Communications
Development Manager,
Philips



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Summary

When the Mobile Communications Division of Philips Semiconductors in Switzerland was faced with the task of designing a new 2.5G/3G system-on-a-chip for wireless applications, the problems typical for complex SoCs had to be tackled. The team was looking for alternatives to the traditional debug and verification flow because the design would probably exceed the capabilities of the existing hardware emulator. A new approach was hard to find, however, because the solution should be usable by three co-operating facilities of the group. Furthermore, the project had to meet a very aggressive deadline, and only limited resources were available.

Having foreseen this situation for quite a while, Philips had already conducted a feasibility study in the area of rapid prototyping and investigated how to map complex designs to multiple FPGAs. “Manually partitioning a design to different FPGAs is extremely error-prone, very complex, and inherently risky,” explains Rolf Singer, mobile communications development manager. “We therefore looked for tools that could straightforwardly partition a design to multiple FPGAs.” This tool was also supposed to be the central element of the different capabilities offered by the projected verification solution.

SoC Design Requires a New Verification Approach

Today’s system-on-a-chip (SoC) devices for communications systems represent a tremendous challenge for the designer because of their twofold complexity. First, they include large-scale functions consisting of proprietary circuits, third-party IP, or reused circuit blocks from previous development projects. Second, circuits designed for mobile devices tend to include many independent clock domains in order to reduce their power consumption and to ensure a long battery life. Hardware emulation used to be the most popular solution for this task. However, emulators are sophisticated hardware systems which are expensive and also require large budgets for operation and maintenance.

Different Approaches and Their Pros and Cons

The new solution should offer lower cost and more flexibility, as well as stability and the potential for future integration with a rapid-prototyping solution. Four alternative solutions were discussed at the beginning of the project:

- Total elimination of emulation and rapid prototyping from the development project — This would result in risks that would have dramatic influence on project planning and the time to market. This approach was therefore ruled out.

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- Prototyping without emulation — If verification was exclusively based on rapid prototyping, the result would require up-front work due to the highly asynchronous, power optimized designs of the communications world. If such a design is mapped to an FPGA, less detailed information is available about how the circuits are implemented. In addition when the project decision was made, no convenient debugging tools for FPGAs were available. Therefore, this solution was not as useful for designs that may not have matured yet, making it unsuitable as well.
- Emulation without rapid prototyping — A solution based exclusively on emulation cannot be justified from a financial point of view.
- Emulation and rapid prototyping combined — This approach offered the best of two worlds. For verification purposes, the design is partitioned into stable sections (e.g. IP or reused circuit blocks) and newer, less mature sections. IP or reused blocks do not require any additional detailed debugging. They can be mapped to an ASIC without any difficulty. In the emulator, this leaves additional space for the less mature sections that can be straightforwardly debugged in the emulator.

Emulation and Rapid Prototyping Combined

The fourth approach utilizes a prototyping board as a capacity-enhancement solution for the emulator. As the IP blocks used in the design are already verified to a large extent, they can be transferred to the prototyping board whose missing debugging functions do not play a significant role. On the other hand, the newly designed, less stable parts of the project are assigned to the emulation system where convenient tools can be used for debugging.

As a key prerequisite for this solution, a special partitioning tool must be available. Following extensive evaluation, Philips decided to use the Certify® tool from Synopsys' Synplicity Business Group. Certify software can transparently partition a design without any tool-specific modifications to the code, targeting not only multiple FPGAs but different kinds of target hardware as well.

Results

The first verification project executed following the introduction of this approach was a success. According to Rolf Singer, "The integration between the emulator and the prototyping board was achieved in one week instead of four weeks as was originally scheduled." Apart from the hardware environment, this is achieved by the tool's transparent and stable operation during the partitioning process. Says Singer, "It is easy to see where the circuits are placed and to which FPGA they are assigned. In addition, the Certify software can automate large sections of the design even though manual intervention is always possible. With the exception of VHDL configurations, the Certify product was able to use the unmodified code originally written for the design. No modifications dictated by the FPGA or the tool were necessary for the partitioning process or for RTL synthesis."

This integrated solution is extensively used by Philips. "It operates reliably and smoothly and offers much better performance than any simulator," comments Singer. Equally important, the approach described here enabled a cost reduction of several hundreds of thousands of dollars compared to a pure emulation solution. Only two engineers are required for operating and maintaining the entire hardware infrastructure and the synthesis flow including the Certify software. In the meantime, the flow operates almost automatically, requiring manual intervention only in case of very intricate problems.

Partitioning the designs to an emulator and a prototyping section had additional advantages. "Assigning the IP blocks to FPGAs has shortened the turnaround time of design modifications, because compiler runs are much shorter using an emulator," says Singer. "We now expect one to two hours for one compiler run instead of four to six hours in the past. In one specific case, we were able to finish a new release every week in the final phase. Because minor problems occurred in each release, three to four compiler runs per day were sometimes necessary. This would have been impossible to handle with the longer run times of the past."

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