

SYNOPSYS®

Predictable Success

“Prototyping with FPGAs is a good solution for the problems that arise in designing our ASICs, and the Certify software approach is a good way to go, mainly due to the automated partitioning. For large, complex designs, it is less work, effort, and money versus hand partitioning. This is why we use the Certify product exclusively in this specific part of our design flow.”

Tom Hilgerdenaar,
Project Team Leader
for Systems Engineering,
Handheld Group,
ATI Technologies



Synplicity®

Simply Better Results

Success with the Synopsys® Synplicity® Business Group and ATI Technologies

Certify® Success Story

Summary

ATI Technologies used the Certify® ASIC prototyping solution from Synopsys' Synplicity Business Group to synthesize and verify the design of a graphics chip for next-generation handheld devices. The Certify tool partitioned the complex design among four FPGAs and filled a vital role in debugging the design. FPGA prototyping with the Certify product provided many advantages over traditional hardware emulation — running code up to 100 times faster, allowing prototype boards to be built at one-tenth the cost, FPGA prototyping also helped identify timing-sensitive bugs that could have prevented first silicon success.

Now ATI has adopted the Identify® RTL debugger as well, further fortifying its arsenal of debugging tools. The Identify tool's speed, power, and ease of use will help the company bring new graphics chip technology to the market even faster.

Certify ASIC Prototyping Partitions Design Too Large for One FPGA

ATI is a world leader in delivering leading-edge solutions to educate, empower, and entertain audiences worldwide. The company is best known for the innovative 3D graphics solutions that it designs and manufactures for desktops, laptops, workstations, video game consoles, and other devices. Another important target industry is handheld devices, an emerging market for ATI. The firm's technology plays a key role in advanced PDAs and cell phones — generating top-quality 2D graphics while keeping power consumption to an absolute minimum

In fall of 2002, ATI began developing a key ASIC that will power next-generation PDAs and cell phones. ATI wanted to prototype the design using FPGAs before committing to an ASIC. Not only did FPGA prototyping reduce the risk of ASIC failure, but it allowed ATI to create multiple implementations of the design on printed circuit boards early in the design-manufacturing process. Equipped with these boards, internal groups and third parties could commence software development early, and marketing and sales could begin conducting customer demonstrations. If ATI had had to wait for ASICs to be produced, these important time-to-market advantages would have been lost.

However, the design was too large to fit in a single Xilinx Virtex 6000 FPGA, the target device. Therefore, ATI needed a FPGA synthesis solution that was capable of automatically partitioning the design across four FPGAs. “We had a choice of approaches, but the Certify product from Synplicity was clearly the right solution for us,” said Tom Hilgerdenaar, Project Team Leader for Systems Engineering in the Handheld Group. “Since hardware synthesis is a core technology for Synplicity, we believe the Certify tool is

Certify Success Story

central to their strategy and will therefore be very well supported over the long term. I'd had positive experiences with Synplify Pro® solution in the past and I knew the quality of Synplicity products."

Certify Solution Provides Massive Speed Advantages While Saving Costs

ATI acquired the Certify product and immediately went to work. One engineer addressed the ASIC code partitioning while Hilgerdenaar designed the board that contained the four FPGAs. "The Certify tool has a number of useful features that eased the process. It displays the number of input/output connections that each FPGA requires, for example, which made it easy to maintain balance among the four devices and avoid exceeding pin number limitations. We also found it straightforward to move portions of the code around between devices," he reported.

In spring of 2003, ATI completed the initial design and proceeded to manufacture 25 copies of the board, some of which were shipped to developers and marketing groups. "The Certify software approach allowed us to avoid the high cost of traditional hardware emulation, and therefore, it was economically practical to make all the prototype boards we needed," said Hilgerdenaar. "Furthermore, the code runs up to a hundred times faster, which served our development and demonstrations purposes much better."

Debugging Expedited by Two Synplicity Products

As the design proceeded through prototyping, ATI experienced another benefit of the Certify tool. Using the Certify product as a verification tool, ATI was able to find many bugs quickly that would

have taken far longer using emulators. Furthermore, since the Certify product allows us to emulate much closer to real time, it was able to identify timing-related bugs that might have eluded emulator verification. "Certify product verification is a better way to test than emulation. You're using real hardware instead of models. It's closer to the real world," said Hilgerdenaar. "It's entirely possible that we caught bugs with the Certify software approach that otherwise would have made it through to ASIC manufacturing." ATI experienced first silicon success when the foundry began delivering ASICs in August.

Debugging FPGAs in the future will be even easier because of ATI's recent acquisition of the Identify tool. "It's an easy to use, very fast debugger that points directly to the source code — which you can't do with a logic analyzer," said Hilgerdenaar. "The Identify product provides virtually infinite visibility into a design."

The Handheld Group's designs are taxing the limits of the Certify technology in many ways — multiple combinatorial feedback paths among FPGAs, for instance. Therefore, many occasions arose to call on Synplicity for support. "Synplicity was responsive whenever an issue came up," said Hilgerdenaar. "Prototyping with FPGAs is a good solution for the problems that arise in designing our ASICs, and the Certify software approach is a good way to go, mainly due to the automated partitioning. For large complex designs it is less work, effort, and money versus hand partitioning," concluded Hilgerdenaar. "This is why we use the Certify product exclusively in this specific part of our design flow."

SYNOPSYS®
Predictable Success

Synopsys, Inc.
Synplicity Business Group
600 West California Avenue
Sunnyvale, CA 94086 USA
www.synplicity.com