VCS Xprop
Increasing the Efficiency of X-related Simulation and Debug

Overview
Verilog and VHDL are commonly used to model digital designs. Designers use RTL constructs to describe hardware behaviors. However, certain RTL simulation semantics are insufficient to accurately model hardware behavior. Therefore, simulation results are either too optimistic or pessimistic compared to actual hardware behavior.

Verilog and VHDL RTL simulators ignore the uncertainty of X-valued control signals and assign predictable output values because of these semantic limitations. As a result, RTL simulations often fail to detect design problems related to the lack of X-propagation. However, these same design problems can be detected in gate-level simulations, and often many gate-level simulations must be run only to debug X-related issues. With the new X-propagation support at RTL in VCS®, engineers can now save time and effort debugging differences in X-modeling between RTL and gate-level simulation results.

VCS Xprop
VCS® Xprop is designed to help find X-related issues at RTL and reduce the requirement for lengthy gate-level simulations. The simulation semantics of conditional constructs in both HDL languages, Verilog and VHDL, are insufficient to accurately model the ambiguity inherent in un-initialized registers and power-on reset values. These issues are particularly problematic when the indeterminate states that are modeled as ‘X’ values become control expressions.

One of the most common sources of simulation differences highlighted when VCS Xprop is enabled is incorrect initialization sequences. The behavior is typically caused by a reset or clock signal transitioning from 0 to X, 1 to X or vice-versa. If a flip-flop is sensitive to the rising edge of its clock signal, an X to 1 transition will trigger the flip-flop and pass the value from input to output when coded using the Verilog posedge or the traditional VHDL flip-flop behavioral code: clk’event and clk’1. Conversely, if the flip-flop is coded using the VHDL rising_edge(event) construct, the flip-flop will not load a new value.

Effectively, the Verilog construct as well as one VHDL construct consider the X to 1 transition as true while the other VHDL construct considers it as false. However, in a VCS Xprop simulation, the same clock transition will cause the flip-flop to merge the input and output, possibly resulting in an unknown value. Hence, to effectively load new values onto a flip-flop, you must ensure that clock signals have valid and stable values, which will be shown in RTL run through a VCS Xprop-enabled simulation.

Figure 1: Verilog Semantics with and without VCS Xprop
VCS Xprop Scope and Support

VCS Xprop is user-controllable in scope allowing partial instrumentation of the design. A user can also configure VCS Xprop to user different merge algorithms (providing support more or less pessimistic semantics). VCS Xprop works with all testbench and high-level description languages supported by VCS (SystemVerilog, SystemC/C++ and VHDL). VCS technologies including coverage, debug, and native low power are also supported with a VCS Xprop simulation as well as VCS in co-simulation mode including AMS co-simulation.

VCS Xprop Debug

When a bug is found in VCS Xprop-enabled simulations, the user may still dump waveforms. Debugging an X-related simulation mismatch actually becomes easier at RTL rather than at gate level because RTL descriptions are closer to the actual functional intent of a circuit. There are different methods to debug RTL simulation failures, but typically, when VCS Xprop is enabled, the regression is run, a regression or test failure is identified, the test is rerun with waveform dumping enabled, the user goes to the point of test failure (usually identified by an assertion or monitor failure), and the user leverages signal tracing to identify the origin of the X and root cause the problem.

VCS Xprop Improves the Efficiency of X-related Debug

VCS Xprop has been shown to be effective on dozens of commercial designs and has been in production since 2010. VCS Xprop provides a methodology to debug X-related issues quickly in large designs with no additional tools or recoding required. Please contact your account team for more information.

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