Formality® is an equivalence-checking solution that uses formal, static techniques to determine if two versions of a design are functionally equivalent. Formality includes an intuitive, flow-based user interface to streamline the verification process. The IEEE-1801 IEEE Standard for Design and Verification of Low Power Integrated Circuits (UPF) adds additional constraints on the design affecting synthesis and verification. Using Formality with the proper methodology, you can ensure that a hierarchical bottom verification flow will find design modifications which cause unwanted changes in behavior.

**Traditional Non-Power-Aware Hierarchical Verification**

In a non-power-aware hierarchical design flow, sub-blocks are synthesized and verified individually. When these sub-blocks are used at the parent level of the design, the logic function remains a black box. There is no boundary optimization across the hierarchical boundaries of previously synthesized sub-blocks for top level synthesis and optimization and during verification. This approach ensures the function of the design at all levels has not changed, maintains a manageable design size and achieves efficient formal verification turn-around time.

![Figure 1: Non-power-aware verification](image)

**Hierarchical Verification in the Presence of UPF**

When UPF is applied to a design, it can change the behavior of existing blocks anywhere in the design. It adds power functionality to the design, including power switches, isolation cells and retention registers. These constructs can affect the functional behavior of the design outside of the block where the UPF is loaded, and the lower levels of hierarchy. For example, if a single top level UPF file adds isolation and retention to lower level sub-blocks, the independent verification of a sub-blocks is invalidated, breaking the traditional hierarchical verification flow.
Fundamental Requirements for Safe and Accurate Hierarchical Verification

If a sub-block is to be black boxed, it cannot reference objects outside of its own hierarchy and the proper power constraints must be captured to allow complete verification at the parent level. Any external information (constraints) that can impact the functionality of the level being verified must be fully specified and must also be visible and validated when verifying the “parent” or sub-block designs.

For a complete bottom up hierarchical UPF flow, the UPF should not reference or create objects outside of the scope that will be visible to the design being synthesized and verified. Each sub-block to be synthesized and verified should have self-contained UPF which does not modify or reference anything outside of its own hierarchy. This block level UPF approach allows for Formality to capture all of the power constraints that apply to the sub-blocks in a new kind black box called a Formality Power Model (FPM).
Capturing Hierarchical Power Constraints in Formality

If sub-block is to be black boxed the proper power constraints must be captured to allow complete verification at the parent level. These constraints are necessary for correct corruption and may be required for isolation policies that will be implemented outside of the block. In a low power UPF design these constraints include the relationship between boundary logic ports and the related supplies that affect those ports.

After a low power design has been read into Formality, a low power model can be created. Each model contains the necessary constraints so that it can be used in the parent level verification.

A traditional black box has no power constraints therefore it cannot be used to determine isolation or proper shut down behavior at the parent level. The Formality Power Model is a complete representation of the block level design as a black box with the related power constraints captured at the ports. The Formality Power Model is used during the parent level verification in place of the traditional black box model. Both the reference and implementation models should be read into the parent design, instead of reading the original designs as black box interface only models.
Using the Formality Power Model ensures a complete and accurate verification using a hierarchical design flow which cannot be achieved using traditional black box models.