Engineering the APX2500 Verification Methodology for Low Power

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Nvidia APX-2500: The World's Lowest Power, High Definition Video and Graphics Computer on a Chip

- **NVIDIA® HD AVP**
  - High Definition Audio Video Processor
  - Ultra Low Power 3d graphics
Design Challenges

• **Stringent Power Constraints**
  – Stringent power constraints at 250mW
  – Conventional power techniques no longer enough
  – Complex power management scheme requires LP design expertise and an advanced design and verification solution

• **Shrinking Time To Market**
  – Extremely tight design schedule
Attributes of a desirable verification solution

• **Power Spec and Library**
  – Concise, unambiguous and comprehensive
  – Accurate voltage aware modeling of Voltage regulators and power switches

• **Dynamic & Static Verification**
  – Low-power verification solution scaleable across projects
  – Accurate voltage aware dynamic verification
  – Comprehensive static verification with no false positives
Handicaps Of Traditional Solutions

• Methodology
  – Power is an after-thought

• Flow
  – Flow must be “enhanced” into a power-aware design flow with home-grown scripts which is a challenge to create and maintain

• Tapeout Risk
  – Issues too late into the design flow
  – Script guards against known mechanisms of failure – What about the “unknown – unknowns”? – One does not want to learn this the hard way!!!
Synopsys Low-Power Verification Solution

- **MVSIM/MVRC**
  - Unified infrastructure for both static and dynamic verification
  - A structured silicon proven solution scaleable across projects
  - Automated assertions to catch errors upfront
  - Solution used
    - **MVSIM** from Synopsys used for low-power dynamic verification
    - **MVRC** from Synopsys used for low-power static verification
Conclusion

• MVSIM/MVRC identified design bugs missed by internal solutions, saving months of design cycle time

• MVSIM/MVRC helped in
  – Eliminating risk from the tapeout schedule
  – Identifying issues early in the design flow at RTL stage saving significant design cycle time and avoiding respins
  – Sign-off check at netlist stage ensuring silicon success
  – Establish a structured low-power verification methodology in existing design flow, scaleable across projects
  – Augmented existing in-house power design flows

• First pass success of power management silicon with Synopsys’ MVSIM and MVRC