Overview

CustomExplorer™ Ultra provides a comprehensive regression and analysis environment to increase verification productivity and streamline the verification process for analog and mixed-signal designs. The combination of CustomExplorer Ultra and Synopsys’ CustomSim™/VCS® mixed-signal verification solution provides design teams with a high-performance, productive mixed-signal simulation and regression management environment for complex SoC verification.

Introduction

CustomExplorer Ultra is an advanced regression and analysis environment for mixed-signal verification. This high-productivity environment combines simulation setup and job control (including LSF and Grid support), multiple testbenches and corners configurations, results analysis, waveform comparison, and debug to significantly reduce the complexity of the mixed-signal verification tasks.

Regression Automation

CustomExplorer Ultra is seamlessly integrated with the CustomSim/VCS mixed-signal verification solution. Multiple testbench and corner configurations can easily be set up and simulation jobs are automatically queued and submitted to the server farm. Simulation job distribution and monitoring gives real-time status of multiple jobs running on multiple machines, providing quick feedback if problems are detected during simulation.

Advanced Analysis and Debug

Simulation results are collected, processed and presented in a spreadsheet-style display, providing an easy-to-read visual summary of the verification tests. Pass/fail results are indicated in the display, and the results can be filtered by design, design variables, equation results, or equation expressions. The unique Waveform Compare technology in CustomExplorer Ultra can be used to compare simulation results to a known-good waveform, saving considerable analysis time. The CustomExplorer Ultra debug environment offers complete SPICE linting, design hierarchy file browsing and signal tracing, as well as cross-probing between netlists, waveforms, and interactively-generated connection visualization for rapid debugging. CustomExplorer Ultra is integrated with Custom WaveView (included), enabling waveform cross-probing and sophisticated waveform measurements. Together, these features aid designers in rapidly performing customized advanced analyses in a powerful design verification and debugging environment for analog and mixed-signal designs.

Heterogeneous Netlists Assembly

Netlists can be imported from a variety of heterogeneous sources and assembled into a single simulation netlist for verification using the configuration manager; SPICE, Verilog, Verilog-A, Verilog-AMS, and SystemVerilog formats are supported. CustomExplorer Ultra’s ability to assemble heterogeneous netlists from multiple sources greatly enhances the automation of mixed-signal verification.
AMS Design Import
Imports multiple netlists from a variety of sources and formats, including: SPICE, FastSPICE, Verilog-A, Verilog-D, Verilog-AMS, and SystemVerilog (see Figure 1).

Schematic Import and Cross-probing
Custom Designer schematics (as well as other third-party schematics) can be linked to CustomExplorer Ultra directly from the schematic environment. Schematics may be fully cross-probed with all of CustomExplorer Ultra’s views.

Design Configuration
The CustomExplorer Ultra Hierarchy Browser allows quick access to the most complex hierarchy design data. The Hierarchy Browser allows traversing of the design hierarchy, display signal, element list, and tracing connections contained in the hierarchy. These views work in concert to provide rapid access to all of the contents of the design hierarchy including the associated file hierarchy containing the design (see Figure 2). In addition to browsing, the Design Browser has a powerful search function, allowing the user to find design components in the hierarchy based on string, signal, instance and module names.

Corner Setup
Simulation corners are easily set up in a spreadsheet form with access to all design variables. A set of corners can be uniquely created for each test configuration, giving the user a highly flexible and efficient way to specify test regressions (see Figure 3).

Simulation Setup
Simulation setup, including corners, design variables, measures, probes, simulator options and multiple testbench configurations is easily managed in the Simulation Setup (see Figure 4). All simulator setup and options can be saved for future use. Simulation setup supports:
- CustomSim/VCS
- CustomSim
- HSPICE

Job Control
Once the corners and testbench configurations are set up, simulations are queued and sent to the server farm (see Figures 5 and 6). Simulation job distribution (using Grid or LFS) and monitoring gives a real-time status of multiple jobs running on multiple machines and helps warn of problems.
quickly. Results are automatically collected for analysis.

**Results Analysis**
After simulation results are collected, they are presented in a spreadsheet-style display (see Figure 7). Pass/fail results are indicated and the results can also be filtered by design, design variables, equation results or equation string (expression). The Results Analyzer can be used to view simulation results as the simulation is running (real time) to verify results early in the simulation. Test parameters can be adjusted on-the-fly as well. Waveform Compare can also be used to compare simulation results to a known-good waveform. All results can be browsed as well as cross-probed between the displayed views. If an error is found, the feature set of CustomExplorer Ultra can be used for debugging.

**Debugging**

**SourceView and ConnectionView**
The SourceView and ConnectionView shows the contents of the SPICE netlist and creates a visualization of the connections contained within the netlist (see Figure 8).

**SourceView**
The SourceView displays the hierarchical content of the SPICE netlist, allowing the designer to query the contents of a design or cell. Selecting a subcircuit in the SourceView displays the contents of that subcircuit as well as displaying the interface pins and netnames, and parameters in the ConnectionView.

**ConnectionView**
The ConnectionView creates design connectivity visualization of the object selected in the Hierarchy Browser. Included in the diagram are the name of the object, its terminal names and the nets that connect to it. In the case of subcircuits, the internal net names are also displayed, making it easy to follow nets up and down the hierarchy through subcircuit boundaries. Custom Explorer Ultra’s Net Tracer can also be used to follow changing netnames with ease through the design’s hierarchy.

**Signal Tracing**
Signal flow can be traced in both SourceView and ConnectionView. In SourceView, the statements representing a selected net are highlighted and can be traced
subsequently. In ConnectionView, devices or subcircuits connecting a selected signal are displayed and new connections can be displayed for pins/ports of the connected elements.

For instance, Custom WaveView can read in the analog results of an HSPICE simulation, convert those waveforms to digital (single- or multi-bit with user-selectable thresholds) and export those results for use in a digital simulation.

Full cross-probing is supported between both CustomExplorer Ultra and Custom WaveView.

**Other Utilities**

*Hierarchal Netlist Flatten and Export*

Hierarchal netlists can be flattened and exported to tools that require flat netlist views. The hierarchy information is preserved via net names in the flat netlist.

*Source Waveform Preview*

Stimuli statements (Pulse, PWL, Sine, Exp or SFFM) statements can be extracted from netlists and displayed prior to simulations to verify their correctness.

*Parameter Reports*

A final report on all parameters in a netlist can be produced show their final values as passed to simulation.

*Total Device Area Reports*

The widths and lengths of transistors in netlists can be extracted and reported to help verify correct netlist construction. This capability helps eliminate errors like missing unit values that would result in one-meter transistors (rather than 1 micron) or 10-Farad capacitors (rather than 10 femtoFarads).

*HSPICE .Measure Statement Extraction and Replay*

CustomExplorer Ultra contains the ability to scan a netlist and extract out all HSPICE .Measure statements and save them in a file. These statements retain their full design hierarchy and can be modified and replayed against existing simulation results. This capability eliminates lost simulation time when the designer determines, after a simulation, that an additional .Measure needs to be performed, or when a given .Measure was incorrect during the simulation. In the latter case, the simulation does not need to be rerun as the incorrect .Measure can be fixed and replayed against the results, saving time and effort.

*Batch Waveform Compare*

A powerful capability in CustomExplorer Ultra is the Batch Waveform Compare utility. This utility allows designers to compare two sets of simulation runs in batch and produce a text report of the differences. The Batch Waveform Compare system uses a simple rules file that controls the comparisons. Users can define what signals are to be compared and the tolerances of the comparisons. Using sample-based comparison techniques, the Batch Waveform Compare utility compares golden-to-target simulation results and supports both analog and digital waveforms. This capability helps eliminate the vast majority of manual “eyeballing” of analog or digital signals. Users have reported reducing as much as one full week of manual effort to 15 minutes for analyzing 100 analog waveforms.

*CustomSim Circuit Check Error Display*

CustomExplorer Ultra can import and display the error report generated by CustomSim’s Circuit Check (CCK) function.

Once a CCK error report is loaded into CustomExplorer Ultra, you can browse the circuit check errors in the CCK Errors window. Users can...
select a particular device and see the detailed connectivity information in the CustomExplorer Ultra Connection View, as well as managing the display by collapsing or expanding the CCK Report and by masking or unmasking the CCK Report at the command level, the tag level or the individual device level. Selecting an individual device allows both the Source View and the Connection View to be cross-probed. Clicking on a particular signal with tracing capability enabled allows the user to do step-by-step signal tracing, which is very convenient.

**Extensible and Open**

CustomExplorer Ultra is open and extensible and can be controlled in both GUI or Batch mode with scripting. The GUI is also extensible, allowing CAD teams to craft custom measurements and provide them across their organizations through the regular menu system.

**Regression Scripting with the Analysis Command Environment (ACE)**

The Analysis Command Environment (ACE) is a Tcl-based extension language that provides near-complete control of CustomExplorer Ultra. The ACE scripting environment contains hundreds of functions and can control the GUI, the waveform panels, the menu system or the measurement capabilities of either tool. Often used by CAD teams to extend the tools, the ACE scripting capability can also be used to perform Regression Scripting allowing designers to make changes to their design and then replay a wide variety of analyses in batch mode, freeing the designer to work on other aspects of the design. Encapsulating these analyses also means sharing best design practices across an organization improving quality and simplifying the collection of data for design reviews.

**Industry Standard Design Platform Integrations**

CustomExplorer Ultra is also integrated into industry-standard design platforms to help maximize designer productivity during the design phase. A native integration of this tool into Synopsys’ Galaxy Custom Designer® system helps form a complete environment for analog block authoring in a single platform for both cell-based and custom design. Other design platform integrations include:

- Cadence Design Systems: Virtuoso® Composer and ADE
- JEDAT: Asca Circuit Design and Debugging Environment
- Mentor Graphics: Design Architect® IC
- SpringSoft: Laker™ Custom Layout Automation System
Supported File Formats
CustomExplorer Ultra provides support for over 45 different file formats giving it the highest support of simulation file formats in the industry.

- Supported Simulator Formats
  - Synopsys
    - CustomSim and CustomSim FT (HSIM, XA and NanoSim – WDF, WDB, .Out and Vector)
    - HSPICE and HSPICE RF (.Tr0, .Ac0, .Sw0… – Binary and ASCII)
    - VCS (VCD and VPD)
    - Saber (AI/PL – Binary and ASCII)
  - Cadence Design Systems
    - Spectre (PSF, WSF – Binary and ASCII)
    - UltraSim (PSF, WSF – Binary and ASCII)
    - PSPICE (DAT)
    - Incisive (VCD)
  - Mentor Graphics
    - ModelSim (WLF)
    - Eldo (COU 4.3, 4.7 and Tr0)
    - ADMS (WDB and JWDB)
    - ADiT (Tr0 and Tb0)
    - HyperLynx (CSV)
  - Others
    - Agilent ADS (.ds – Binary and TouchStone S-Parameters – ASCII)
    - CSDF (ASCII)
    - Novas FSDB (Binary)
    - Legend (Tr0 Derivative)
    - SmartSPICE (Raw Derivative)
    - Five proprietary simulator formats are also available – please contact Synopsys

- Data Formats
  - IBIS Models
  - Tektronix Agilent and Lecroy Scope Data
  - Text table data and Comma Separated Values (CSV)

Table 1: CustomExplorer Family Products and Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>CustomExplorer Ultra</th>
<th>CustomExplorer</th>
<th>Custom WaveView</th>
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<tbody>
<tr>
<td>Configuration management</td>
<td>✔</td>
<td></td>
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<tr>
<td>Corners setup</td>
<td>✔</td>
<td></td>
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<tr>
<td>Simulation job control</td>
<td>✔</td>
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<td>Results analysis</td>
<td>✔</td>
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<td>AMS debugger</td>
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<tr>
<td>SPICE debugger</td>
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<td>✔</td>
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<tr>
<td>Waveform compare</td>
<td>✔</td>
<td>✔</td>
<td>(option)</td>
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<tr>
<td>tcl Scripting</td>
<td>✔</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Waveform display</td>
<td>✔</td>
<td>✔</td>
<td></td>
</tr>
</tbody>
</table>

- Supported Simulator Formats
  - Synopsys
    - ModelSim (WLF)
    - Eldo (COU 4.3, 4.7 and Tr0)
    - ADMS (WDB and JWDB)
    - ADiT (Tr0 and Tb0)
    - HyperLynx (CSV)
  - Cadence Design Systems
    - Spectre (PSF, WSF – Binary and ASCII)
    - UltraSim (PSF, WSF – Binary and ASCII)
    - PSPICE (DAT)
    - Incisive (VCD)
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- Data Formats
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  - Text table data and Comma Separated Values (CSV)

- Supported Netlist Formats
  - Synopsys HSPICE
  - DSPF
  - Cadence Spectre and CDL
  - Mentor Graphics Eldo
  - Standard SPICE

Platform Support
- Solaris 32- and 64-bit
- Red Hat Enterprise Linux version 4 and 5 (AS, ES, WS)
- SUSE Linux 9.0 and 10.0 and 5 (AS, ES, WS) 9.0 and 10.0