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DESIGN FOR MANUFACTURING: SIMULATION

Bringing Manufacturing Into Design through TCAD

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ABSTRACT

In implementing design-for-manufacturability (DFM) and design-for-yield (DFY) methodologies, it is necessary to go beyond layout printability issues and consider process variability. Technology CAD (TCAD) refers to the use of computer simulations to model semiconductor process and device behaviors. It addresses process variability by complementing silicon data with accurate process and device models based on calibrated simulations of the actual wafer fabrication steps. Since overall circuit performance is greatly affected by the increased variability at the 65 nm node and below, TCAD can help IC designers optimize performance and yield around the expected process variability. This offers significant savings in time and money to semiconductor vendors.

This article demonstrates how TCAD has evolved over time from an R and D to a manufacturing tool. We will show how IC designers can simulate a number of critical effects which only physics-based TCAD tools can replicate, thus enabling faster time to market and lower cost. By extending DFM and DFY beyond printability issues into a complete variability-aware process and device architecture, TCAD provides the required bidirectional link between design and manufacturing.

INTRODUCTION

Over the past decade, TCAD has become essential for developing and optimizing semiconductor technologies ranging from nano-scale microprocessors to large-scale, high-voltage power devices. With increasing computer power, TCAD tools are being used more efficiently for exploring new device architectures and optimizing process flows. Beyond the traditional use for research and technology development, TCAD has been increasingly used in manufacturing for advanced process control and parametric yield improvement. When leveraged to its full extent, TCAD can be extended further to help designers assess the impact of the process on chip performance by bringing manufacturing knowledge into design.

In this article, we start by describing the traditional use of TCAD for research and technology development to explore technology options and optimize process flow and device performance. Then, we will discuss how manufacturing engineers benefit from using TCAD to implement advanced process control and improve parametric yield. Lastly, we will present a new concept of using TCAD simulation-based models in design tools.

TCAD FOR R AND D AND TECHNOLOGY DEVELOPMENT

Each technology generation driving higher density and performance adds increasing complexity. Process architects must wrestle with integrating new materials and device structures into the process. This results in new physical effects such as process-induced stress, statistical dopant fluctuations, spatial quantization and non-equilibrium transport. In the past, many of these effects could have been neglected, but they are now primary considerations in developing a new process technology. This trend drives the need for sophisticated simulation tools that can efficiently point to the right options for technology during the development phase. These tools provide technology development with the physical insight to optimize processes for performance and yield. Without these tools, engineers would be forced to rely on large numbers of experimental wafers, impacting development cost and time to market.

Intense competition in the IC industry has shortened the product life cycle. From product conception to market introduction, the average time is less than 18 months. In some cases, the market has completely disappeared if a product is delayed by three months. In order to be profitable, a new product must not only meet time-to-market constraints but also must reach the target yield at the start of volume production. TCAD simulations, which complement experimental silicon, provide a more comprehensive way to characterize technologies and optimize their performance, thereby reducing the number of re-spins and delivering high-quality products sooner rather than later.

According to the International Technology Roadmap for Semiconductors, technology development costs can be reduced as much as 40 percent by using TCAD. This is significant considering the rising costs of product development. Today, a 300 mm R and D wafer running through a production fab can cost more than $20,000 and new fabs cost in excess of $3 billion. TCAD is the optimal tool for research engineers to explore complex technology options such as the right combination of gate and dielectric materials needed to meet device performance specifications. With TCAD, researchers can narrow options through simulations before running actual

experiments in the R and D lab. Once the technology choices are made, technologists can use TCAD simulations to complement experimental runs for integrating process modules, optimizing performance and improving manufacturability before transferring the technology to manufacturing. More and more semiconductor companies are taking full advantage of the predictive power of TCAD to reduce cost and time in product development.

TCAD FOR IMPROVING MANUFACTURABILITY AND YIELD

After the process is transferred into manufacturing, a whole new set of challenges arises. With shrinking feature dimensions, parametric variability has become a dominant yield loss component. Parametric sensitivity to process variability is expected to worsen at 65 nm and below. In addition, ever-increasing analog and mixed-signal contents in SOC designs have strongly impacted parametric yield. This trend has spurred the need for innovative advanced process control methodologies that rely on an improved understanding of the correlation between process variables and parametric parameters.

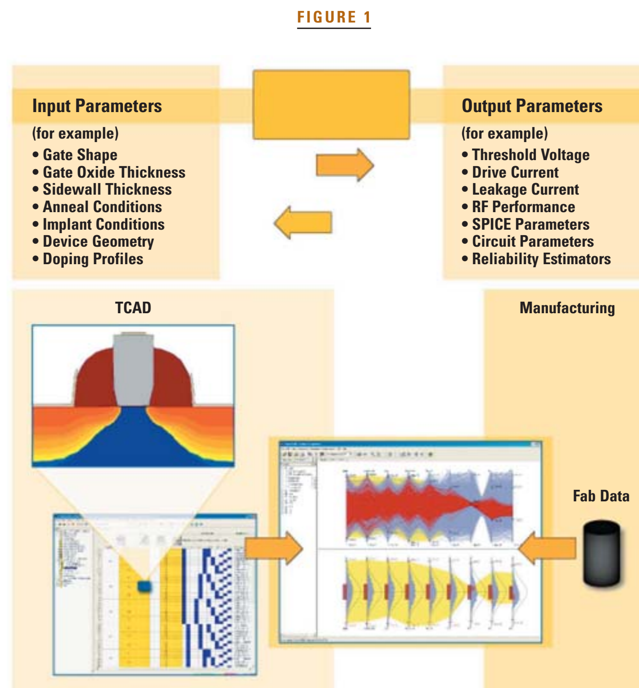
With its physical basis, TCAD is fully capable of capturing detailed process effects on parametric yield parameters. A well-characterized TCAD flow can be used as the basis for generating statistical models that encapsulate key process-to-device correlations through a set of computationally-efficient process compact models (PCM). Figure 1 shows the relationships between input (process) and output (electrical or parametric yield) parameters captured in PCM through statistical modeling. As illustrated in Figure 2, using PCM, manufacturing engineers can analyze process sensitivity, re-center the process and identify key process steps to increase overall parametric yield and implement advanced process control for improved manufacturability. This TCAD-for-manufacturing (TFM) flow effectively strengthens the connection between technology development and manufacturing, and represents an important new way for deriving value from TCAD tools to improve manufacturability and parametric yield.

TCAD FOR LINKING MANUFACTURING WITH DESIGN

For years, design engineers have been relying on two key pieces of information for designing chips: design rules and SPICE models. The design rules define the spacing between edges of polygons in the same mask layer or between mask layers such as poly line spacing or metal overlaps of contacts. These rules have been set by lithography limits including feature resolution and layer alignment or by electrical limits such as leakage or breakdown of the electrically-active layers in the devices. The SPICE models predict the current or the charge between terminals as a function of the applied voltage between the terminals and are needed for circuit simulation. Both design rules and SPICE models are simplified information of the process and devices, intended for transferring only as much manufacturing information to the design tools as is needed.

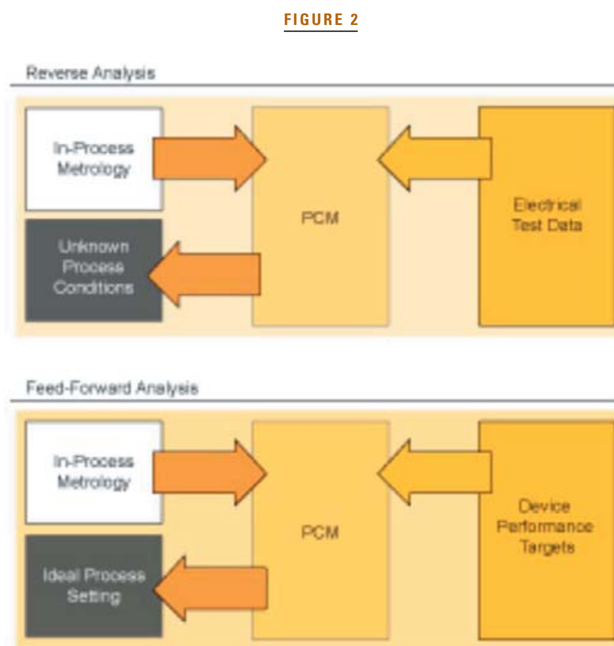
As features shrink, some of the simplifying assumptions about processes and devices are no longer valid and the exact physics of the lithography and process effects have to be incorporated into the design flow. One way is to add more design rules to include many more edges than those of immediate neighbors; another is to make the rules more context-sensitive. As an example, because of lithography proximity effects, the spacing between a line edge and a perpendicular line is defined as a function of the number of neighbors surrounding the edge. A similar situation arises with SPICE models. For previous technology nodes, the transistor characteristics were primarily

FIGURE 1



Process compact models capture the relationships between process parameters and device performance characteristics for manufacturing engineers to perform advanced process control and parametric yield analysis.

FIGURE 2

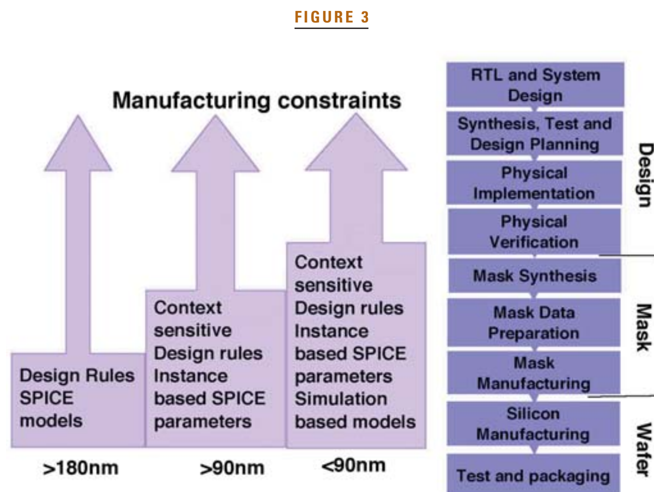


PCM can be used to predict device performance and conduct reverse or feed-forward analysis to assess yield performance.

defined by the gate length and width, both of which can be easily extracted from the physical layout. Beyond the 180 nm node, the transistor characteristics are also influenced by the size of the "diffusion island" and location of the gate in these islands because of mechanical stress from the isolation. In order to account for this effect, extra layout-based parameters have been added to the SPICE models. With further scaling, these techniques have to be extended to include the results of physical simulations into the models and the physical verification flow. Figure 3 shows the evolution of design for manufacturing (DFM) with technology generations and the need for more accurate modeling.

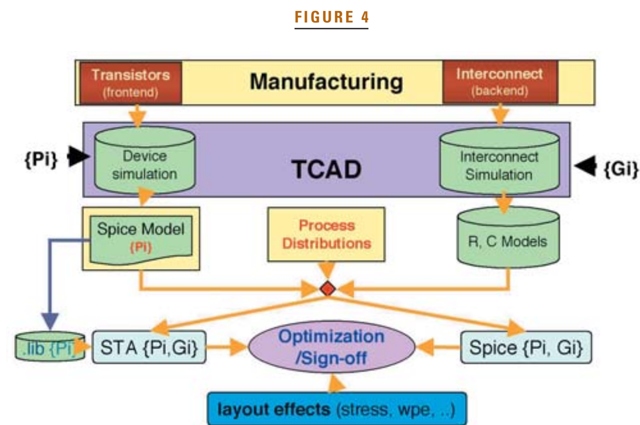
The following gives three examples of how TCAD simulation-based models can be used to assess variability in device, layout and parametric on design, thereby bringing manufacturing knowledge into design tools and driving this new DFM paradigm.

FIGURE 3



Evolution of DFM with each technology node and the information that is fed into the design to manufacturing flow. The sophistication of the design rules and the SPICE models increases with each successive technology node. Simulation-based modeling will have to be used for technology nodes below 90 nm.

FIGURE 4



Flow chart showing how TCAD simulations of the process, device and interconnect are used to create models that can allow front end (Pi) and backend (Gi) process variables to be input to design tools such as a static timing analyzer (STA). In addition, layout-related effects such as stress and well proximity effects (WPE) are also made part of the physical verification flow for final sign-off.

DEVICE VARIABILITY

Most designs are based on nominal values of the device and interconnect characteristics, and the functionality of the design is checked at different process corners to account for variations in the manufacturing process. There are two sources of device variability – layout and process. The first is related to variations of electrical characteristics with specific location on the chip, primarily due to the proximity of other patterns. Examples of this are changes in line width due to proximity effects, changes in mobility due to stress from adjoining patterns, and changes in metal line thickness due to local pattern density fluctuations. The second source of variability arises from process variations from wafer to wafer and also across the wafer. Examples of this are variations in implant dose, line width due to difference in focus or exposure, and metal thickness due to differences in CMP polishing rate across the wafer.

In the past, these two sources of device variability were combined to define the overall performance variation of the design. However, the layout-dependent part for recent technologies is sufficiently large that it needs to be accounted for in the critical parts of the design as part of the overall design flow. Otherwise, it may not be possible to meet the design specifications or achieve the performance benefits of a new technology node. In the case of process-related variability, the effects of the different process steps have in the past been lumped together in an overall device variability model such as the range of I_{dsat} or V_t. But it is now important to assess the effect of each individual process step on the specific parameters of the device. Through the use of calibrated TCAD simulations, models accounting for device variability due to layout and process can be included in design tools to assess their impact on performance. The flow chart for the design using these methods is shown in Figure 4.

LAYOUT DEPENDENT VARIABILITY

A major contributor to layout-dependent device variability is mechanical stress which affects carrier mobility, drive current and threshold voltage. The mechanical stress arises from the surrounding shallow trench isolation (STI). Currently, the effect of STI is taken into account though a length of diffusion (LOD) model that modifies the SPICE parameters depending on the internal layout of the transistor – namely the length of the diffusion rectangle and the position of the gate relative to the edge. This approach has to be extended to account for the fact that the range of the stress in silicon is around 2 microns and hence the characteristics are affected by diffusion patterns within a radius of 2 microns of the transistor. The effect of layout on performance is illustrated in Figure 5, which shows instances of ring oscillators with sparse and dense layouts. The frequency difference between the two layouts is about 15 percent.

Three-dimensional (3D) TCAD simulation tools can be used to calculate the stress in the transistor channel for different layouts. Based on extensive simulations, a set of compact models that can accurately estimate the stresses for different

configurations is determined. These are linked to a polygon processing engine to create an EDA tool that can analyze the change in characteristics for all the transistors in a large block.

PARAMETRIC VARIABILITY

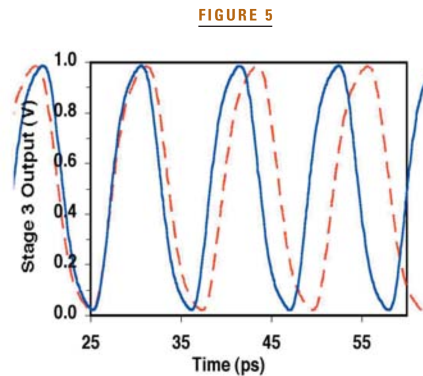
Spice models with various corner cases are traditionally the only link between manufacturing and design. In order to simulate process variations, the standard is to impose somewhat artificial statistical or systematic distributions on the SPICE model parameters. This approach, however, suffers from several fundamental flaws. First, the actual SPICE model parameters may deviate far from their underlying physics, as they often end up fitting parameters to silicon data. Second, the key SPICE parameters are generally correlated with each other because major manufacturing steps such as halo implant and annealing temperature cause global changes in device properties. The device characteristics such as threshold voltage (V_{th}) and subthreshold leakage (I_{off}) seldom change independently of each other. It is therefore erroneous to treat them as statistically independent variables. Dealing with correlated variables in statistical analysis would drastically complicate the modeling efforts. Finally, the SPICE parameters cannot be directly linked to any one specific process parameter, so even if the simulations reveal potential problems with the circuits, there is no direct way to relate them back to specific process conditions. In other words, there is no common language to communicate between manufacturing and design.

However, successful DFM requires that manufacturing information be accessible to design. By combining calibrated TCAD simulations with a global SPICE extraction strategy, it is possible to create self-consistent process-dependent compact SPICE models, with process parameter variations as explicit variables. This methodology brings manufacturing to design so that measurable process variations in the manufacturing line can be fed into design while the design sensitivity to process can be fed back to manufacturing.

Calibrated TCAD flows ensure accuracy of the simulation against silicon, whereas the modeling flow brings the process parameters (Pi), such as implant dose, spike temperature, gate critical dimension (CD) and gate oxidation temperature into the SPICE models. As a result, circuit responses to specific process parameter variations can be simulated using the compact SPICE model.

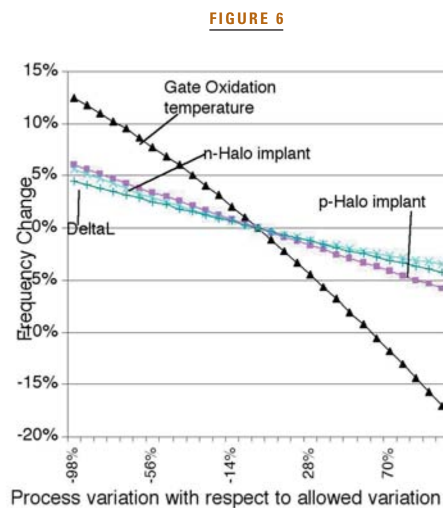
Figure 6 shows the deviation of ring oscillator frequency with variations in halo implant dose, gate oxidation temperature, the change in gate length (deltaL), and V_t adjust implant dose for a typical 90 nm process. The ring oscillator is constructed with 21 stages of 2-input NAND gates, with one of the inputs (control signal) tied high. The frequency of the ring oscillator under nominal process conditions is found to be 66 MHz. Gate oxidation temperature, n-halo implant dose, deltaL and p-halo implant dosage are observed to have significant impact on the frequency of the ring oscillator, with the degree of impact in that order.

FIGURE 5



Layout of individual inverters in ring oscillators and the change in frequency due to layout.

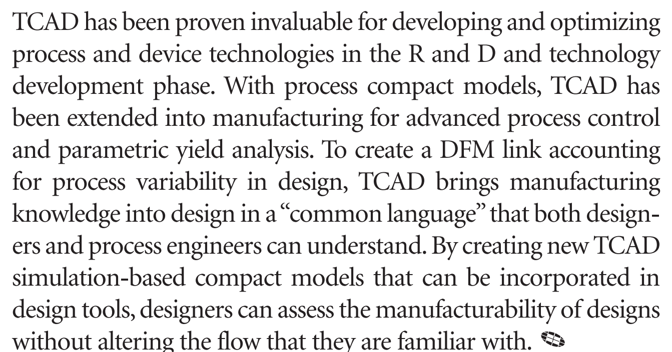
FIGURE 6



Frequency variation of 21 stage 2-input NAND oscillators as a function of process parameter variation.

SUMMARY

TCAD has been proven invaluable for developing and optimizing process and device technologies in the R and D and technology development phase. With process compact models, TCAD has been extended into manufacturing for advanced process control and parametric yield analysis. To create a DFM link accounting for process variability in design, TCAD brings manufacturing knowledge into design in a "common language" that both designers and process engineers can understand. By creating new TCAD simulation-based compact models that can be incorporated in design tools, designers can assess the manufacturability of designs without altering the flow that they are familiar with.



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