

Raphael

Interconnect Analysis Tool

Overview

Raphael is a collection of 2D and 3D field solvers and interfaces for interconnect analysis and modeling. Raphael is designed to simulate the electrical and thermal effects of today's complex on-chip interconnect. Through Raphael's easy-to-use graphical user interface (GUI), process technology data are entered and the critical interconnect structures are automatically generated and characterized for capacitance.

The performance of today's deep submicron silicon technologies is dominated by the parasitic capacitance, resistance, and inductance of the interconnect structures. Critical design issues—timing, power, noise and reliability—require accurate and robust interconnect models. Raphael satisfies this critical industry need by rigorously simulating interconnect capacitance, resistance, and inductance using its industry-standard field solvers and interfaces.

Benefits

- Analyze complex on-chip interconnect structures including effect of process variation
- Create a parasitic database to study the effects of design rule changes
- Generate accurate capacitance rules for layout parameter extraction (LPE) tools
- Extract interconnect capacitance and resistance of design library cells and SRAM cells
- Extract inductance and resistance of wirebonds and on-chip spiral inductors

Technology Characterization with the Raphael Parasitics Database

Raphael uses a highly-automated flow to generate a comprehensive database of capacitance models for a given technology (Figure 1). Guided by an easy-to-use GUI, the user initially specifies an interconnect technology file that describes the thicknesses and physical attributes of the conductor and dielectric layers (Figure 2).

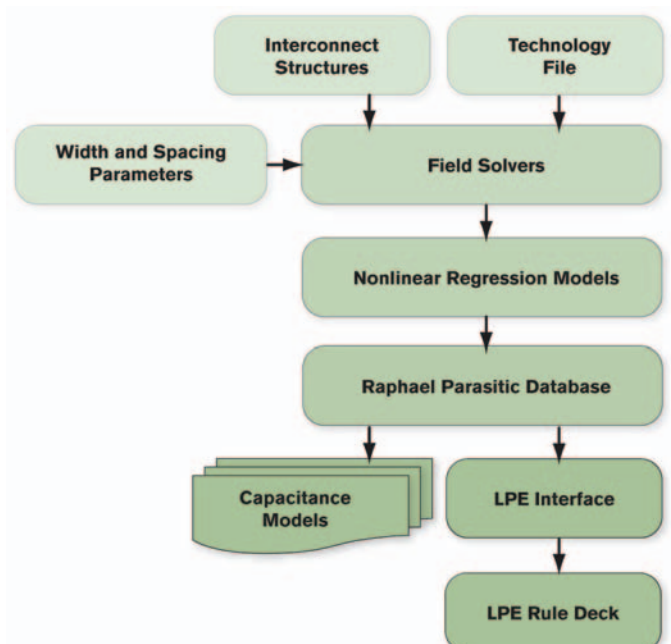


Figure 1. Raphael makes it convenient to generate a parasitic database for a specific technology. The flow includes a link to calibrate LPE tool rule decks.

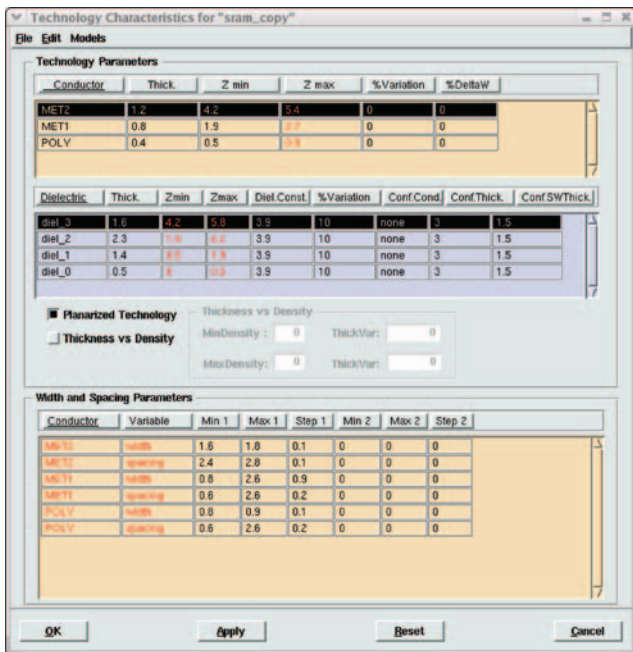


Figure 2. Technology characteristics are defined by entering information about the conductors and dielectrics comprising the interconnect stack.

In keeping with the latest technologies, Raphael includes support for conformal dielectrics and trapezoidal conductors. A set of generic 2D and 3D interconnect structures, representative of interconnect patterns occurring in designs, and the allowed ranges of interconnect widths and spacings are then defined (Figure 3).

Using this information, Raphael automatically generates hundreds or even thousands of input files for the capacitance solvers by permuting the allowed widths and spacings over the generic interconnect structures. Raphael then launches the appropriate field solver, 2D or 3D depending on the structure, to obtain the capacitance solution for all the structures.

To make all this data manageable, Raphael fits nonlinear regression models to the numerical solutions using well-known default equations. Optionally, user-defined equations can be substituted.

The outcome of this flow, which can be fully automated, is the Raphael Parasitics Database (RPD), an accurate and flexible representation of the capacitance characteristics of a given technology which process and device engineers can use to establish process specifications and design rules (Figure 4).

Using the Raphael Parasitics Database to Calibrate LPE Tools

CAD engineers can use Raphael to calibrate LPE tools. Using the accurate capacitance models stored in the RPD, rule decks for Mentor Graphics' XCalibre and ICextract, and Cadence's Dracula and Diva, can be created using a LPE tool interface utility (Figure 5). This integrated solution allows IC designers to improve extraction accuracy for full chip and critical net analysis.

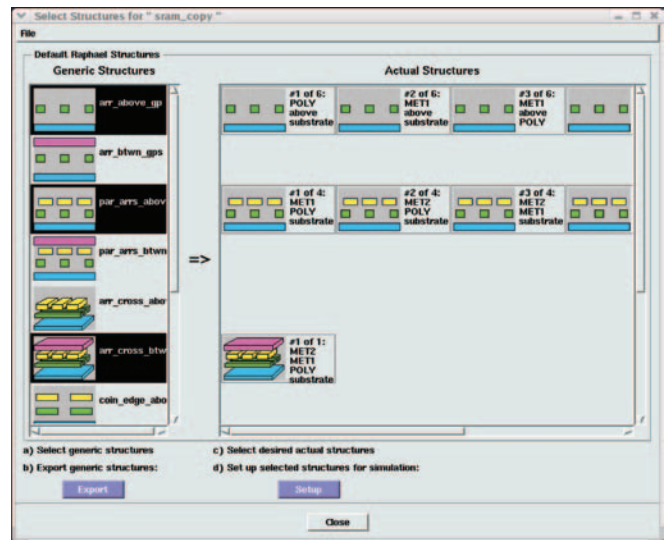


Figure 3. The user can select from a wide range of generic interconnect structures for field-solver simulations. The generation of input files is done automatically.

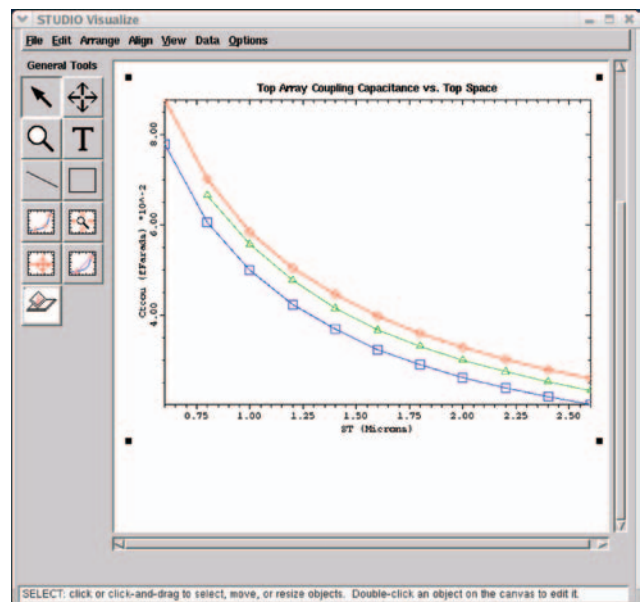


Figure 4. Capacitance-versus-spacing plots help engineers analyze the effect of process or design rule changes.

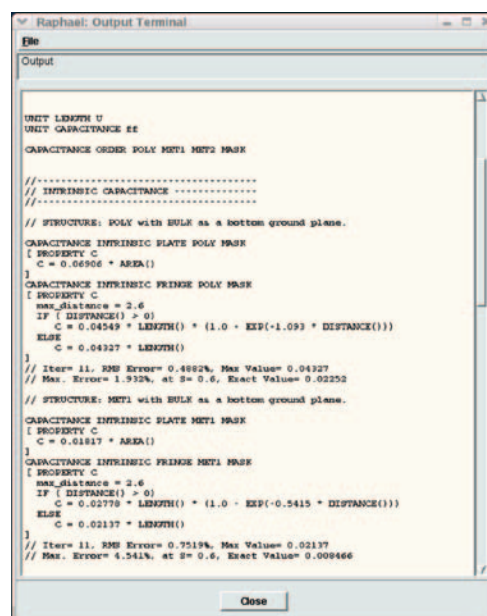


Figure 5. The LPE link generates capacitance rules which can be included in rule checks.

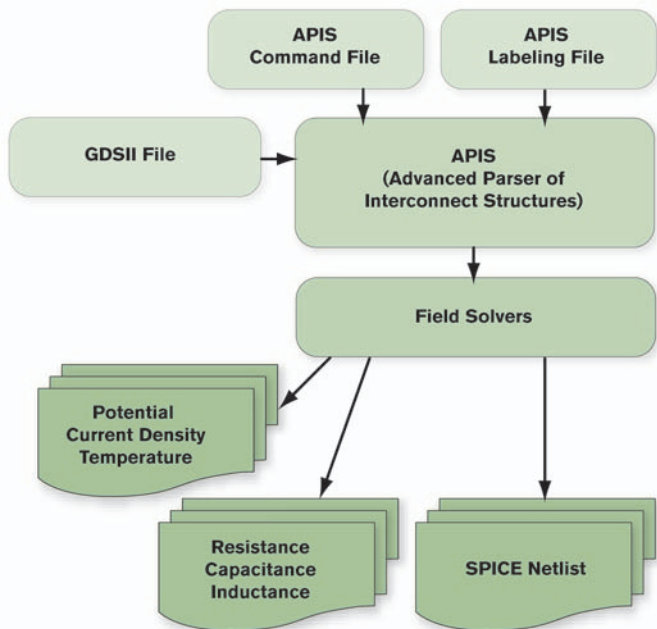


Figure 6. Raphael reads GDS-II mask files and merges them with technology information to create input files for the 3D solvers.

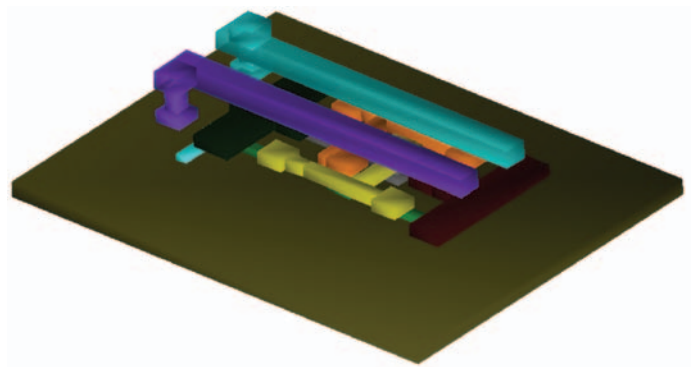


Figure 7. Raphael offers SRAM cell generated from GDS-II mask file and technology file.

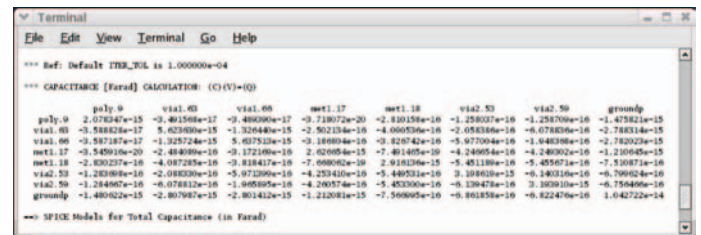


Figure 8. Raphael generates capacitance matrix output.

Using Raphael in Technology Development

In addition, Raphael is used to analyze detailed interconnect structures as required during technology development. The Advanced Parser for Interconnect Structures (APIS) utility combines a GDSII mask file with a technology file to create 3D input files for Raphael's field solvers (Figure 6). With this capability, simulation structures for design library cells, SRAM cells, and on-chip spiral inductors can be easily generated (Figure 7).

A link with the Synopsys topography simulator, Sentaurus Topography, also is provided to allow engineers to incorporate detailed etching and deposition effects into the interconnect structure.

Raphael's 2D and 3D field solvers then are used to simulate the capacitance, resistance, and inductance of these structures. Internal field variables (e.g., electric potential and field, temperature, and current density) also can be extracted and visualized, thus providing users with unsurpassed insight into the electro-thermal characteristics of interconnect structures (Figure 8).

Raphael Interconnect Library and SPICE Model Generation

While Raphael provides a great deal of flexibility in creating interconnect structures, engineers sometimes wish to analyze a number of common interconnect structures without going through the process of generating these structures. To address this need, the Raphael Interconnect Library (RIL) allows users to simulate many common structures directly from a predefined menu (Figure 9).

Many simulations can be performed by setting up a table of input values. A typical run not only produces the lumped values for the resistance, capacitance, and inductance but also generates an associated lumped or distributed SPICE netlist (Figure 10).

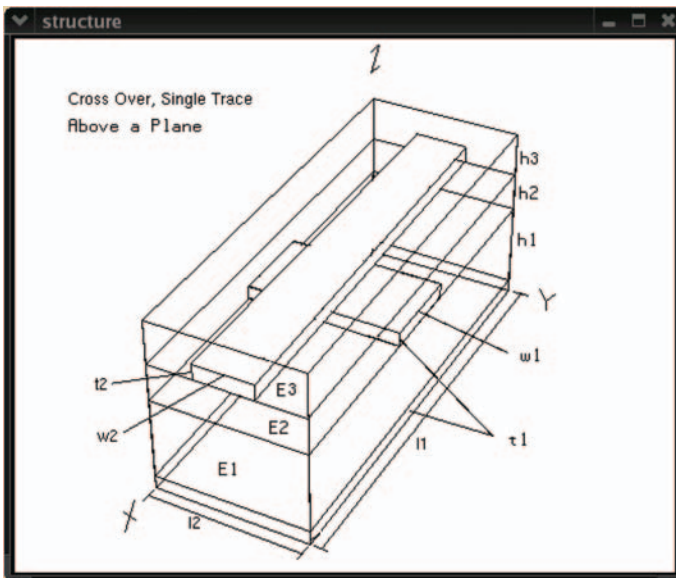


Figure 9. Two cross-over traces are one of many structures that the user can easily set up for simulation by entering only a few parameters.

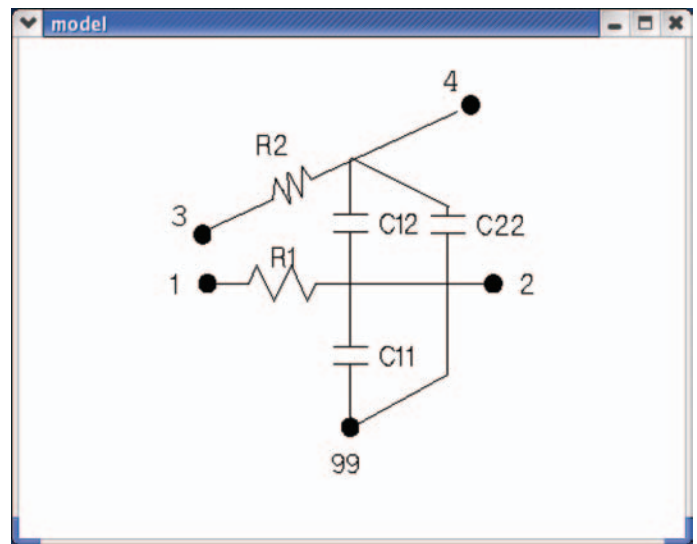


Figure 10. Raphael generates a SPICE model for the cross-over structure.

Features

- Computes 2D/3D interconnect capacitance and resistance using finite-difference solvers
- Computes 2D/3D interconnect capacitance using boundary-element solvers
- Computes 3D resistance and inductance with skin effect using a magnetostatic solver
- Computes electric potential and field, temperature and current density distributions
- Simulates trapezoidal conductors and floating conductors
- Simulates conformal dielectric layers, including anisotropic dielectric constant

Interfaces

- Includes Taurus Layout, a cell-level GDSII viewer
- Sentaurus Workbench Visualization and Taurus Visual for visualization of output results
- Sentaurus Topography for incorporating detailed interconnect processing steps
- Synopsys' Star-RC, Mentor Graphics xCalibre and ICextract, Cadence Dracula and Diva interfaces for accurate full-chip post layout parameter extraction.

Outputs

- Capacitance, resistance, and inductance matrix
- Nonlinear regression models for generic capacitance structures
- Lumped electrical capacitance, resistance and inductance
- SPICE equivalent circuit netlists for library structures
- Distributions of electric potential and field, current density and temperature
- Rule decks for LPE tools

Visualization Tools

- Sentaurus Workbench Visualization and Taurus Visual (interactive 1D, 2D, and 3D graphical output)
- DPLOT (2D/3D graphical output)

Supported Platforms

- Sun 64-bit, Solaris 9
- IBM RS6000 64-bit, AIX 5.1
- x86 (IA-32) 32-bit, RHEL v3

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