

Simulations provide additional insights into GaN HFET reliability

GaN HFET reliability can be improved by adding field plates to the structures. This is believed to reduce carrier trapping at the surface, but simulations by **Ric Borges, Nelson Braga, Bo Wu** and **Vidas Mickevicius** of Synopsys show that it also decreases the electron temperature and bulk trapping throughout the device.

GaN HFETs are attracting considerable attention as high-power and high-frequency devices for radar, avionics and wireless base-station transmitters, thanks to the unique material properties of III-N material. However, the commercialization of these devices has been hampered by reliability issues that have been attributed to carrier trapping in either the bulk or surface of the device. These problems are being addressed by experimental studies that can produce epitaxy- and processing-related improvements, and simulations that can optimize device design.

Simulations provide key insights into device operation and the degradation mechanisms that affect reliability. They can contain structural details such as layer thicknesses, doping profiles and trap concentrations. The software-based approach can also aid the tailoring of a structure to specific market applications requiring particular performance characteristics, and can be an effective tool for selecting and optimizing the design.

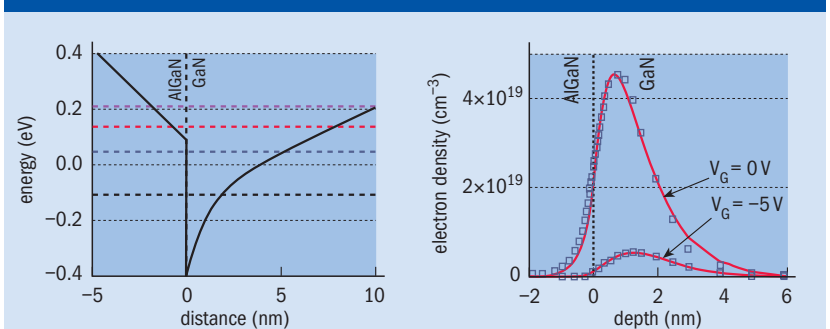
In the silicon industry, process and device simulation – referred to as technology computer-aided design – is widely used to develop and optimize various technologies ranging from highly scaled CMOS to power management, non-volatile memory and image sensors. Over the past decade this approach has also been increasingly used for III-V technologies, and recent advances to III-N devices has promoted the use of simulation for improving GaN HFETs.

Investigating current collapse

At Synopsys we have built the simulator software Sentaurus Device (see “Simulation software” box, opposite, for details) to explore a physical mechanism that is referred to as either current collapse or dispersion, and is defined as the drain current (I_D) degradation under operational or stress conditions. This mechanism limits GaN HFET reliability and is consequently inhibiting device commercialization. However, its origin is still under debate despite the various models that have been proposed, such as electron trapping in the GaN buffer and AlGaIn barrier layers, and at the surface (Binari *et al.* 2002, Vetry *et al.* 2001).

Our simulations can help to understand the nature of current collapse, provide a detailed insight into

Simulation software



The interface between the GaN and AlGaIn layers can confine electrons in the conduction band in four different energy states (see left figure). Although calculations using Schrödinger’s equation can be used to simulate the electron density in the channel at $V_G = 0$ V and $V_G = -5$ V (see right figure, solid line), time savings can be made using the density-gradient approach, which involves a quantum-mechanical correction to the continuity equation (see right figure, square markers).

The simulation of GaN HFETs presents several challenges and needs to cater for the polarized wurtzite crystal structures of AlGaIn, InGaIn and GaN, which have dipoles across the crystal in the [0001] direction. These dipoles can cause spontaneous (pyroelectric) polarization, while pseudomorphic heterostructures fabricated from these III-Ns also have strain-induced (piezoelectric) polarization.

At Synopsys, our software, which can be run on either PCs or workstations, provides a rigorous calculation of the polarization fields from the stress in the structure – including local stress sources such as the gate metal and dielectric passivation – and leads to in-plane polarization vector components. The resulting polarization-induced charges are included in our calculation.

Quantization effects at the AlGaIn/(In)GaIn heterointerface create a two-dimensional electron gas channel. A quantum-mechanical solution is needed to properly account for the electron spatial distribution in this channel. Our model uses a quantum potential correction to the continuity equation, known as density gradient. This closely matches the solution to the full Schrödinger equation (see figure, above right), while improving the simulation’s robustness and providing a five-to-ten fold cut in computational time. Our simulation also accommodates hot-carrier effects and dynamic trapping/detrapping, which is needed to simulate the physical mechanisms behind device degradation.

device operation, and point towards mitigation strategies to avoid current collapse. However, they cannot predict the formation of non-ideal device properties such as traps.

The software has simulated a GaN HFET (see figure 1) with a room-temperature Hall mobility of

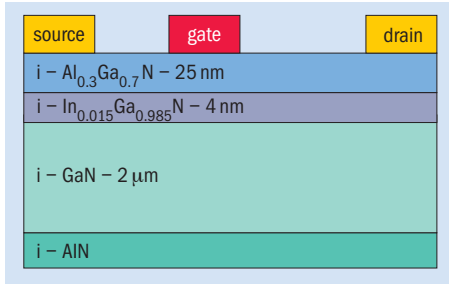


Fig. 1. Our simulations model intrinsically (i)-doped AlGaIn/InGaIn HEMTs with a $5 \times 10^{17} \text{ cm}^{-3}$ trapping density and $\sigma_{Tn} = 1 \times 10^{-15} \text{ cm}^{-2}$ capture cross-section.

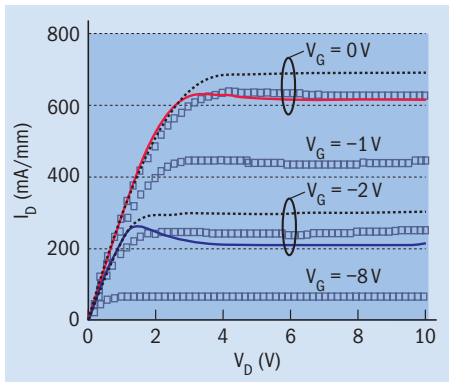


Fig. 2. The hydrodynamic transport model (solid lines) that includes hot-electron effects is a better fit to the experimental data (squares) than the drift-diffusion model (dotted lines). Simulations have only been performed for $V_G = 0$ and -2 V.

The properties of III-Ns

	GaN	InN	AlN
Dielectric constant	9.5	15.3	8.5
Energy gap (eV)	3.47	0.8	6.2
Electron affinity (eV)	3.4	5.8	1.9
Electron mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	1100	2400	300
Electron saturation velocity (cm/s)	1.2×10^7	2.6×10^7	1.5×10^7
Effective conduction band density of states (cm^{-3})	2.65×10^{18}	1.3×10^{18}	4.1×10^{18}
Energy relaxation time (ps)	0.1	0.1	0.1

Table 1. The Synopsis simulations use the room-temperature values for III-Ns that are shown in the table. The values are taken from the work by M E Levinshstein and colleagues (M E Levinshstein *et al.* 2001 *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN and SiGe*, Wiley, New York).

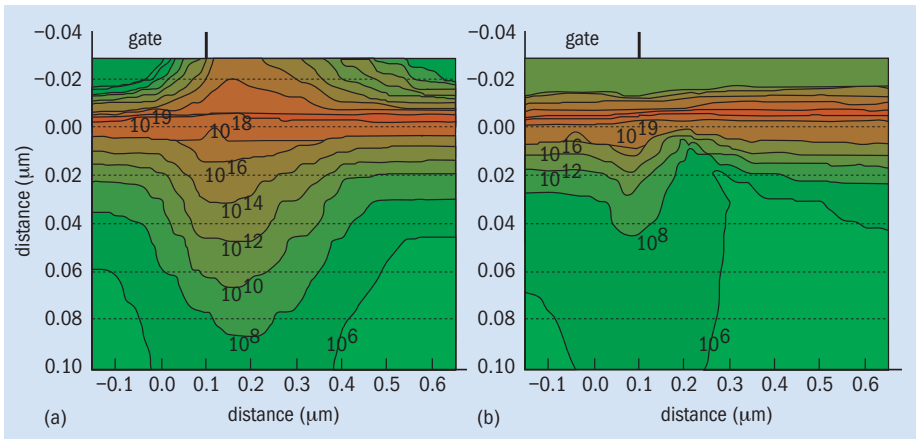


Fig. 3. The simulated electron density map of the cross-section of the AlGaIn/InGaIn HEMT generated using the hydrodynamic model shows that the electrons spread over the AlGaIn barrier into the GaN bulk (a). The simple drift-diffusion model simulation, which does not consider hot-electron effects, confines the electrons to the channel (b).

1100–1200 $\text{cm}^2/\text{V}\cdot\text{s}$ and sheet carrier concentration of $8\text{--}9 \times 10^{12} \text{ cm}^{-2}$ (Braga *et al.* 2004). The calculations used values for the band structure, carrier mobility and saturation velocity of GaN, InN and AlN that are shown in table 1. Interpolation of the corresponding binary parameters provided values for AlGaIn and InGaIn.

Trapping behavior

To investigate trapping behavior and gain insight into the current-collapse mechanisms, we inserted a background of acceptor/electron bulk traps with a density of $N_T = 5 \times 10^{17} \text{ cm}^{-3}$ into our model of this particular device. Since the motivation behind this study is to obtain a qualitative insight, the traps were defined with a single energy level 1 eV above mid-band. However, our simulation software can accommodate multiple trap levels that are commonly ascribed to GaN epitaxial material (see Binari *et al.* 2002) in either the bulk or at the surface.

Using these conditions we could match our simulations of direct-current (DC) I-V characteristics with measured data if we used an interface charge of $1.15 \times 10^{13} \text{ cm}^{-2}$ and an electron saturation velocity that is 40% of the theoretical bulk value. The value used for the interface charge, which equates to a partially relaxed AlGaIn layer, is lower than that associated with theoretically-ideal strain conditions, which would have a value of $1.5\text{--}1.7 \times 10^{13} \text{ cm}^{-2}$. However,

this value is consistent with observations from several experimental groups who have seen a reduction of the piezoelectric component. A reduction in saturation velocity has already been proposed, due to modified scattering of the two-dimensional electron gas (2DEG) at the heterointerface.

We also compared the experimentally-measured DC $I_D\text{--}V_D$ output characteristics with simulations that both ignore and include hot-electron effects (see figure 2). Our drift-diffusion (DD) model assumes that the carriers are in thermal equilibrium with the lattice, while the hydrodynamic hot-electron compatible (HD) model accounts for carrier heating and non-local electric field effects. The measured and simulated curves created with the hydrodynamic model have a decline in their I_D value after the peak – known as a negative differential conductance – that is absent in the curve produced with the DD model. We believe that this feature is not attributable to self-heating (Deng *et al.* 1999), but is in fact evidence for hot-electron capture at bulk traps under sufficiently high drain bias.

The HD model also shows that at large drain biases electrons in the channel are significantly heated and can exit the AlGaIn barrier and then spread toward the GaN bulk – an effect that is not predicted with the DD model (see figure 3). At these high drain biases electrons occupy more traps. This increases the energy of the conduction band under the gate edge located

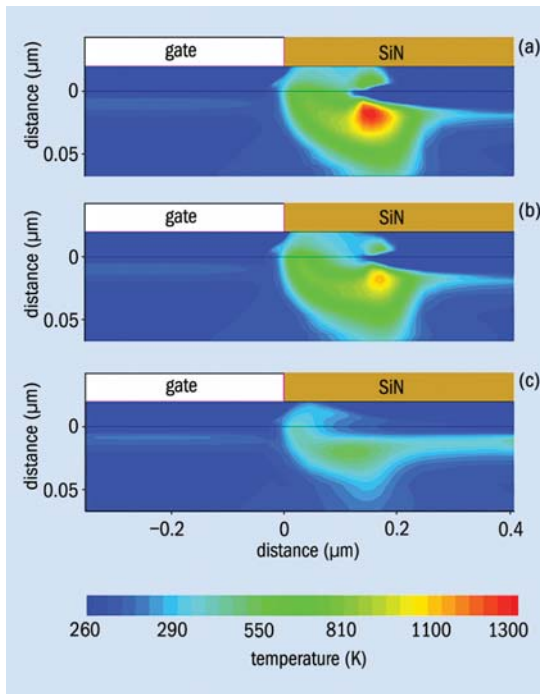


Fig. 4. GaN HEMTs with gate field plates (c) and source field plates (b) have lower electron temperatures near the drain-edge of the gate than comparable devices without a field plate (a). Note that the field plates are not shown in the plots.

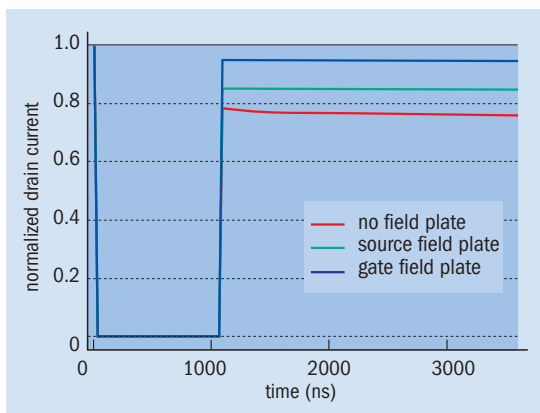


Fig. 5. Transient gate-lag simulations show that the source and gate field-plate structures both aid the recovery of the drain current, and will consequently improve device reliability.

toward the drain, and creates a potential barrier to electron flow.

The loss of electrons from the drain channel, which leads to current collapse, can be prevented by improving the electron confinement in this region. In fact this improvement has already been observed in a AlGaIn/InGaIn/GaN double heterojunction FET structure that features a potential barrier between the InGaIn channel and the underlying GaN layer (Simin *et al.* 2001).

We simulated the effect of the potential barrier on current collapse by carrying out transient simulations at differing indium concentrations that are akin to gate-lag measurements. These HD simulations involve setting the drain voltage to 0.1 V and giving the gate a

1 μs gate pulse from 0 to -5 V, which is then restored back to 0 V. These simulations confirm the improvement in current collapse resulting from the use of InGaIn layers to provide superior channel confinement of the 2DEG.

Field-plate enhancements

One of the most compelling attributes of GaN HFETs is their high-voltage operation, which produces a higher output impedance and wideband impedance matching. Recent work suggests that field-plate structures are effective at reducing current collapse at high voltages (see, for example, *Compound Semiconductor* January/February 2006, p25). This is because field plates reduce the electric field at the drain-edge of the gate, which leads to a lower electron temperature.

We investigated the electron temperature in GaN HFETs with no field plate, a source field plate and a gate field plate. When the device is built without a field plate, hot electrons diffuse into the bulk and are trapped, but when a gate field plate is used, the electron temperature is reduced (see figure 4).

The impact of field plates on current collapse can be assessed with transient simulations. Using conditions identical to those for the transient simulation already described, but with the exception of an increase in the drain voltage to 6 V, revealed that the gate field-plate structure yields an almost complete recovery of the drain current, indicating very small gate lag (see figure 5). This analysis is consistent with reduced hot-electron diffusion and trapping, and shows that the addition of field plates will improve device reliability.

Our hot-electron-based model of current collapse suggests a different mechanism from the “virtual gate” model, which argues that high electric fields at the drain-edge of the gate cause electrons to be injected from the gate into surface traps (Vetry *et al.* 2001). However, since surface trapping of electrons is well known in compound semiconductors, it is plausible that both models play a role in current collapse.

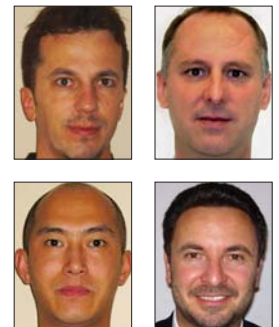
We believe our simulations, which show that field plates and double heterostructures can suppress the hot-electron effects in the bulk region of a transistor, can accurately model device behavior, and are an invaluable tool for optimizing this promising technology toward its eventual commercialization. ¹

Acknowledgments

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