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Options at the 45nm node include

engineered substrates

OVERVIEW Compatibility with existing design methodology dictates the continued use of planar transistors at the 45nm technology node. Engineered substrates, however, offer a way to significantly enhance prior node performance through back integration. Options include a combination of strain enhanced mobility techniques, different gate stack materials, and engineered substrates. Advantages and disadvantages of several feasible planar structures for the 45nm process are assessed. It is shown that engineered substrates could allow current 65nm process technologies to be extended down to 45nm.

Planar MOSFETs have been successfully used from the 1970s down to the 90nm technology node. To be compatible with standard design methodology, however, planar structures need to be used down to the 65nm and 45nm nodes. One major factor affecting the scaling and performance is the overall current drive/unit width of the transistors. The target performance for each technology node is listed in the *International Technology Roadmap for Semiconductors* (*ITRS*) [1]. The focus of this paper is on high-performance logic devices. Process options that are considered include: 1) different gate materials — polysilicon vs. metal; 2) different gate insulator materials; 3) strain engineering — both global (wafer level) and local (process strain); and 4) different engineered substrate options where thin silicon layers are transferred onto silicon substrates.

Extensive evaluation of the options was done using 2D and 3D process and device technology CAD (TCAD) simulation tools [2] that were calibrated based on experimental results from published data and previous technology nodes.

Simulation details

The devices were constructed by simulating a full CMOS process flow using 3D TCAD tools. The process parameters for each node were chosen to meet junction specification listed in the *ITRS*. The isolation scheme used shallow trench isolation (STI). The effect of different gate insulators was modeled by adjusting the effective oxide thickness (EOT). The gate material was either polysilicon or metal. Source and drain (S/D) extensions were formed by low-energy implant of the appropriate species followed by activation.

For the 65nm node, the activation was achieved with a spike anneal, but a scanning laser anneal was used at the 45nm node [3]. The channel and S/D doping are formed by implanting and annealing In+As and As+B for the nMOS and pMOS transistors, respectively. Mechanical stresses were applied to the transistor channel using both intentional and unintentional stress sources. For the nMOS transistors, intentional stress sources were tensile shallow trench isolation (STI), tensile NiSi salicide, and tensile nitride cap layer. For the pMOS transistors, compressive stress was applied by etching away the S/D silicon and epitaxially growing a SiGe layer [4]. Additional stress was applied by using a compressive nitride cap layer [5].

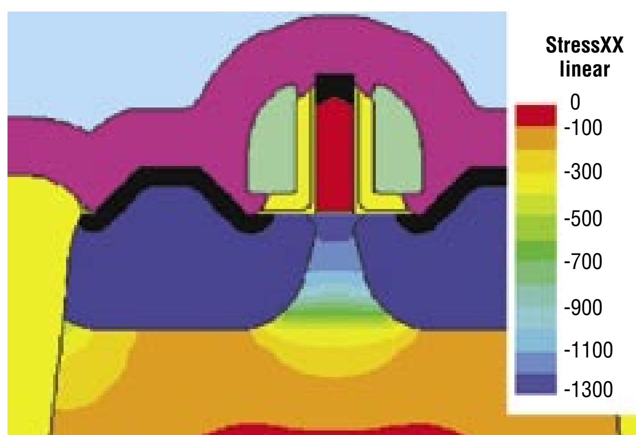

Figure 1. Geometry and stress distribution in a 20nm pMOSFET with elevated SiGe S/D and compressive nitride cap layer. The stress is shown in MPa for the stress component along the channel.

Figure 1 illustrates the simulated structure and stress distribution in a typical 20nm pMOSFET. The cross-section of the nMOSFET is similar except that the pMOSFETs have elevated SiGe S/Ds, while nMOSFETs have a flat silicon S/D.

Device simulation used drift-diffusion approximation with mobilities calibrated to the moderately nitrided gate oxides and polysilicon gates. No mobility adjustments were made for heavily nitrided gate dielectrics or for metal gates. Both polysilcon depletion and quantum mechanical (QM) effects in the polysilicon were accounted for in the case using polysilicon gates. For both polysilicon and metal gates, QM effects in the silicon channel were included. Stress-induced mobility enhancements were based on the piezoresistance model [6].

The dopant activation in polysilicon is $10^{20}cm^{-3}$ for the 65nm node. Enhanced dopant activation of $1.3\times10^{20}cm^{-3}$ can be achieved by scanning laser annealing and is the value used for the 45nm node simulations. In the case of metal gates, two different metals are used for the nMOS and pMOS. The work functions of the individual metals were

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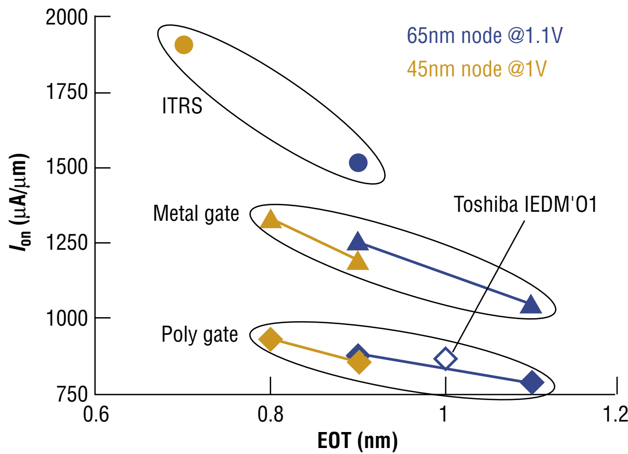

Figure 2. Results for stress-free nMOSFETs with poly and metal gates compared to the *ITRS* requirements. The measured data for a 35nm nMOS is obtained from [7].

chosen to be within 130mV from the conduction and valence bands, respectively, to achieve the target threshold voltages.

The power supply voltage was 1.1V for the 65nm and 1.0V for the 45nm node. Consistent with the *ITRS* specifications, the off-state current I_{off} is fixed at 70nA/µm for the 65nm node, and 100nA/µm for the 45nm node. Physical gate lengths were 30nm and 20nm for the 65nm and 45nm nodes, respectively.

Effect of pure scaling on performance

Figure 2 compares performance of the 65nm and 45nm devices for different EOTs; the results for stress-free devices are shown as a baseline. Devices with the polysilicon gates have drive currents much below the *ITRS* requirements. Shrinking EOT by either increasing the nitride content in the gate oxide or introducing a high-*k* dielectric provide only marginal I_{on} improvements. This is counter to what analytical expressions for I_{on} would predict, but is due to the fact that the device performance is determined by capacitive effective thickness (CET) rather than EOT. In the case of a polysilicon gate, the CET is dominated by the polysilicon depletion rather than by EOT.

Introduction of the metal gate boosts performance by ~40% by eliminating polysilicon depletion if the mobility in the channel is not degraded. It also increases I_{on} sensitivity to the EOT by bringing CET closer to EOT. However, this performance boost is not sufficient to match *ITRS* requirements.

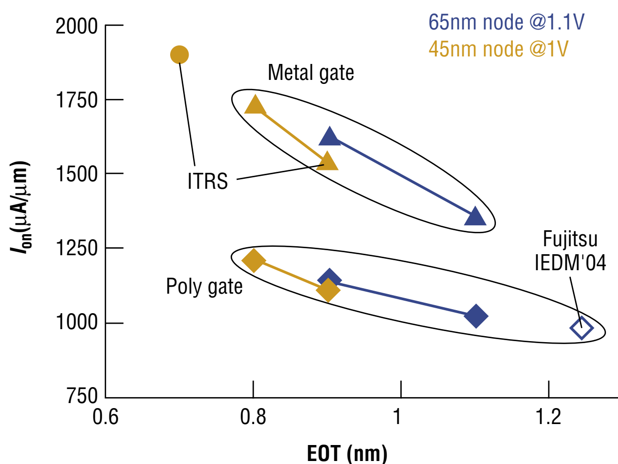

Figure 3. Results for stress-engineered nMOSFETs with poly and metal gates compared to the *ITRS* requirements. The measured data for a 40nm nMOS is from [8].

Stress engineering can significantly enhance the I_{on}/I_{off} ratio [8–11]. By optimizing the stress from each of the stress sources, electron mobility enhancements of up to 72% and hole mobility enhancements of up to 120% can be achieved for 45nm [9]. This translates into I_{on} enhancements of ~36% and 60% for the nMOS and pMOS, respectively.

Figure 3 shows how stress engineered nMOSFETs compare with the *ITRS* specifications for different types of gates. The calculations depicted in Fig. 3 are based on a somewhat conservative 30% stress-induced I_{on} gain. For the polysilicon gate, the stress-induced mobility enhancements fall short of satisfying the *ITRS* requirements. Specifically, I_{on} falls short by ~30% at the 65nm node and by ~40% for the 45nm node. However, when stress enhancement is coupled with metal gates, it is possible to match the *ITRS* requirements.

Another key performance factor for circuits is the transistor delay that is estimated as $\tau = CV/I_{on}$, where C is gate capacitance and V is the supply voltage. **Figure 4** presents the ratios of the transistor delays to the Roadmap specifications.

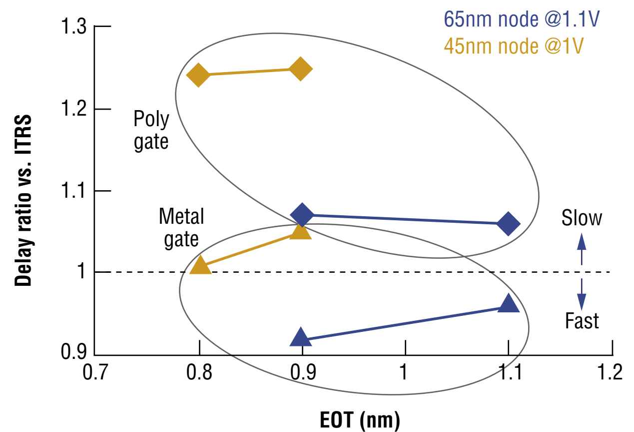

Figure 4. Ratio of stress-engineered transistor delay vs. the *ITRS* spec.

The target ratio on this plot is 1.0 so that results <1.0 satisfy the roadmap, while results above do not. The delay for the 65nm nMOS with the poly gate is 7% short of the *ITRS* requirement, but grows to 23% at the 45nm node. The combination of metal gate and stress engineering meets the requirements.

The conclusion is that the standard bulk nMOS with the poly gate is close to Roadmap requirements for the 65nm node, but it cannot be extended to the 45nm node without a major performance impact. The next section discusses several process options and substrate engineering solutions that can be used to overcome this performance deficit. All of these approaches could also be applied to 65nm and greater nodes for significant additional performance gains.

Options at 45nm

To meet the roadmap requirements for sub-65nm process nodes, modifications to the transistor materials, processes, and substrates are needed, while adoption of nonplanar transistor structures — such as FinFET or tri-gate that introduce significant additional process, design, and technology challenges — can be avoided [12].

Bulk substrate solution

Metal gate with dual workfunctions for nMOS/pMOS. It has been shown that the use of metal gates increases I_{on} of the 20nm-long nMOSFET by ~40% compared to polysilicon gates. Combined with stress-related enhancements, this is enough to meet the *ITRS* requirements at the 45nm node. The introduction of a metal gate eliminates poly depletion and QM effects in the gate and thus reduces CET by ~0.3nm. This significantly improves subthreshold swing and channel control by the gate.

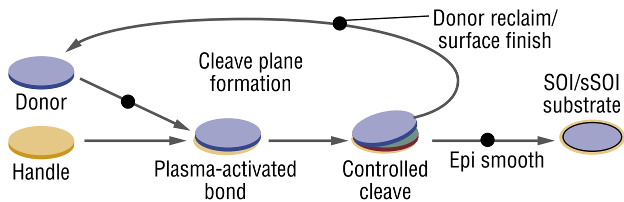

Figure 5. Basic elements of a layer-transfer engineered substrate fabrication process. (Source: SiGen)

Introduction of a metal gate can extend the life of planar devices by another generation or two. Metal gate improves performance of any MOSFET regardless of the specific structure, and therefore should be eventually introduced for bulk or SOI as well as multigate devices. The difference is that bulk devices require two metals with different work functions for the nMOS and pMOS that are close to the conduction and valence band, respectively, whereas thin silicon devices like fully depleted SOI (FDSOI), FinFET, and tri-gate MOSFET require work functions that are close to the mid-gap. This implies that different metals would be needed for bulk devices compared to thin film devices. Difficulties in finding appropriate metals and the cost of integrating these into a process flow may prevent this approach from being used for the 45nm node.

Engineered substrate solutions

FDSOI and hybrid orientation substrate technologies. Recent advances in layer-transfer technologies allow ultrathin SOI and silicon-on-silicon substrates to be manufactured with the required defects and device silicon-layer uniformity specifications for high-yield, deep-submicron process node manufacturing [13–14]. The basic manufacturing steps of a layer-transfer (LT) process are shown in **Fig. 5**. The main steps include cleave plane formation, plasma bonding, mechanical cleave, and noncontact surface epi-smoothing described elsewhere [13–16]. This LT process is flexible enough to allow SOI, multilayer stacked layers, strained film formation, as well as hybrid substrates such as (110) on (100), for example.

These LT processes allow novel transistor structures to be implemented and are becoming available in mass production at 300mm, a requirement for sub-65nm process node integration.

Nine engineered substrate structures were evaluated for their potential to meet the 45nm node requirements. These included SOI, strained SOI, double-layer engineered films and silicon-silicon bonded LT structures. The LT process options included multiple active layers, buried insulator presence and type, film stress (both biaxial and uniaxial), and film transfer rotation/crystal orientation. The evaluation criteria included performance enhancement, cost, complexity, and practical integration to existing and scalable transistor formations processes. The two structures discussed below were considered the most attractive under the imposed constraints.

Fully silicided gate (FUSI) fully depleted silicon-on-insulator (FDSOI) devices. The main benefits of FDSOI are improved transistor subthreshold swing, speed, and power consumption. Metal gates can be obtained in this technology by a complete silicidation of the polysilicon gate after the transistor has been formed (FUSI process).

It was shown [17] that a 20nm FDSOI nMOSFET with a NiSi gate satisfies the *ITRS* requirements for the 45nm node and can be scaled further for several generations beyond. NiSi gates provide work functions that are close to the mid-gap and can be adjusted within several hundred millivolts by using conventional impurities in polysilicon.

Another advantage of FDSOI devices is that they can benefit from a combination of local and global stresses. The effect of biaxial and uniaxial stresses on transistor performance is now starting to be well understood [18]. Both biaxial and uniaxial global stress can be designed within the FDSOI layer-transfer substrate fabrication process to complement local stress approaches. Current global stress approaches generate biaxial stress using relaxed silicon-germanium virtual donor substrates but have weak or nonexistent pMOS mobility improvement and are still considered too defective and costly for use [4]. A new uniaxial global strain process recently announced by SiGen eliminates many of the cost, defect, and pMOS performance issues [19]. The best global stress pattern that can benefit both nMOS and pMOS would be tensile uniaxial stress in the transverse (orthogonal) direction to device current flow [6].

The main challenge with bringing the FUSI FDSOI into production is the ability to provide FDSOI substrates with the required SOI thickness uniformity specifications at a reasonable price.

Bulk devices on hybrid wafer orientation/twisted bonded wafers. The effective carrier mobilities in the MOSFET channels depend on crystallographic orientation of the wafer surface and on the crystallographic orientation of the channel direction [20–22]. The optimum orientations for the nMOS are (100)/<100> for the surface and channel direction, respectively. For the pMOS, the optimum orientations are (110)/<110>.

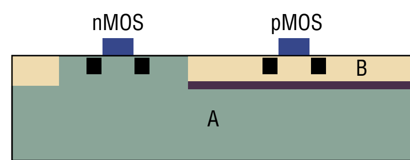

Figure 6. Wafer with hybrid orientations/twists. **A** represents (100) wafer with <100>-channel direction. **B** represents thin silicon layer with surface orientation of (110) and channel directions along <110>.

The advantage of using these optimum orientations instead of the standard (100)/<110> is that the electron mobility can be improved by a factor of 3 [6] by stress engineering and the hole mobility by a factor of 2 using the more beneficial (110) silicon crystal orientation [20–22]. These mobility improvements are sufficient for Roadmap requirements to be met using bulk devices and standard polysilicon gates. **Figure 6** illustrates how these two sets of surface and channel orientations can be combined on a single bulk-like wafer.

The structure is produced with a starting base wafer **A** with (100) surface and the notch placed such that the n-channel transistor channels are aligned with the <100> crystal orientation. A second layer **B** is transferred from a handle wafer with a (110) surface orientation that is twisted relative to wafer **A** such that the p-channel devices have their channels aligned with the <110> crystal orientation.

Both nMOS and pMOS transistors now have the same physical

direction of the channels, even though the silicon for each type is oriented differently. This allows the layout and lithography to stay unchanged. After wafer bonding and layer-transfer of the **B** layer onto the handle wafer **A**, the **B** layer is selectively removed from the n-channel areas by patterning and etching. Selective epitaxial growth is used to bring the surface of the n-channel regions to the same level as the p-channel regions. Global strain is not expected to be possible or effective with this technology due to the relatively thick top silicon layer and the tendency of global strain to relax in low channel-width bulk structures [23]. This approach has the advantage of using the same design tools and the same gate stack materials as at the 65nm node with a slightly modified process flow. The extra cost of the substrate can be obviated by the lower cost of using standard materials.

Conclusion

3D TCAD simulations have been used to efficiently evaluate different process and engineered substrate technology options. Results show that *ITRS* requirements can be satisfied using planar MOS device technologies using three separate process combinations. The first is the use of full metal gate MOS combined with process strain; the main issue in implementation is a lack of suitable choices for gate metallization. The second and third options use FDSOI and hybrid orientation engineered substrate technology to meet *ITRS* requirements in a practical and cost-effective manner. Uniaxial strain is proposed for FDSOI to simultaneously improve nMOS and pMOS device performance. All these approaches could be back-integrated to significantly increase 65nm and greater node performance. ■

Acknowledgments

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