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What designers need to know about TCAD

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Issues with manufacturability and yield are forcing the EDA industry and IC manufacturing to move closer together. In particular, process and device information that affect functionality and yield need to be incorporated into the design technology, addressing more comprehensively issues like Design for Manufacturability (DFM) and Yield (DFY).

Currently DFM focuses mostly on optical proximity correction (OPC), neglecting other factors like process and device variability. In yield terms, this means that the current focus only covers parts of the parametric yield issues. We have to extend our coverage of DFM and redefine it.

The information needed by designers includes layout sensitivities as well as the effect of process variability on the electrical characteristics of devices and interconnects. At the 65nm node the variability will increase significantly as a result of feature scaling, and the introduction of new materials and innovative techniques such as strain engineering.

The current dilemma faced by the EDA industry is that a complete enumeration of manufacturability related rules, requiring a process and device model derived from manufacturing data, is not available until sufficient silicon has been processed. Yet most of the circuit blocks have to be designed with EDA tools before this information is available.

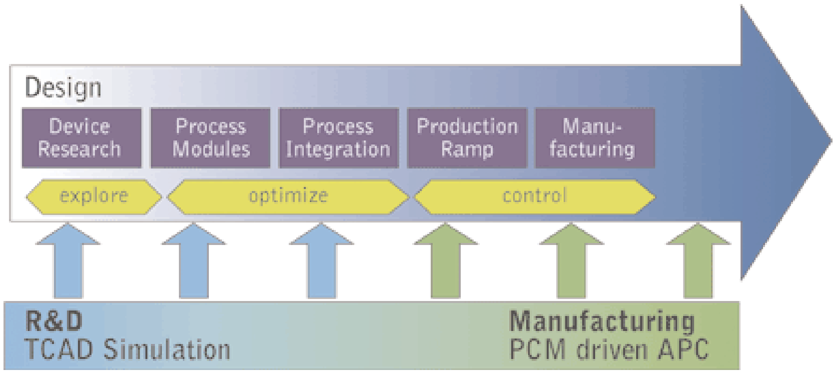

Figure 1 — Evolution of TCAD through the technology cycle. The initial TCAD flows that are used to develop and optimize the process evolve into a calibrated flow that can be used to control the manufacturing flow. The sensitivity of the design to process variability is captured by Process Compact Models (PCM) that can be used in a manufacturing flow for Advanced Process Control (APC) to improve parametric The design phase begins in the early phases of process development.

Enter TCAD

TCAD (Technology CAD) addresses the problems as it complements silicon data with an accurate process and device model based on calibrated simulation. In combination with measurements on wafers, the strength of TCAD lies in the accurate prediction of device and interconnect variability due to layout, as well as random variations in the process, which can then be incorporated into the design tools.

TCAD has developed from a tool that has historically been heavily used in R&D to a tool that can also be used in manufacturing, as illustrated in Figure 1. During process technology development, TCAD models are calibrated to silicon data to accurately characterize key process steps such as shallow junction formation and strain engineering.

The individual process steps are integrated in a complete manufacturing flow, which is also modeled by TCAD. The electrical characteristics of the transistors are simulated and calibrated. TCAD can now be used to study the sensitivity of the transistor characteristics and to optimize process steps to reduce the amount of electrical variability. For example, the halo and extension implants can be optimized to reduce the effect of gate CD variations on leakage power without compromising drive current.

Beyond process and device modeling and optimization, TCAD can be used in the manufacturing line for a process-global advanced process control (APC) targeting parametric product yield for specific designs without the manufacturing engineer having to understand the details of the design. Thus TCAD becomes a tool that is used to control manufacturing steps to meet specific design objectives.

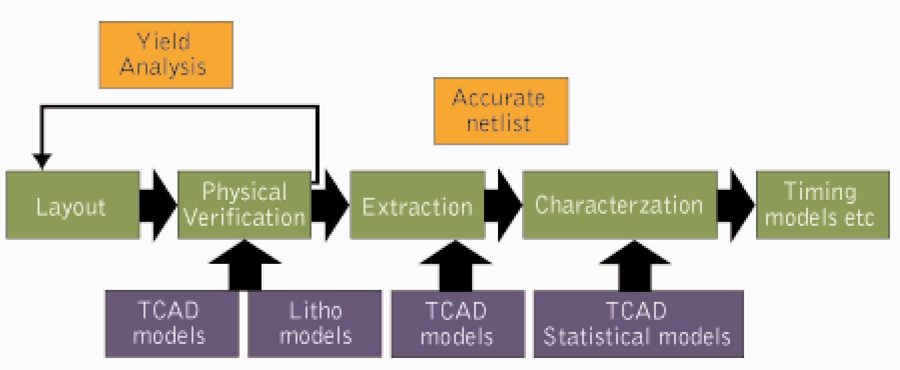

Figure 2 — Flow to create DFM and DFY compatible cell level designs. The physical verification combines TCAD and lithography modeling to assess the parametric yield of the cell . A feedback loop can be used to optimize the layout. TCAD models are then used for accurate netlist extractions followed by statistical characterization of the cells.

TCAD links design technology with manufacturing

DFM and DFY are not a one-way street. In the current situation, DFM and DFY are deadlocked by a mutual dependence of design and manufacturing, through the requirements of:

- Design robustness with respect to manufacturing, and process relevance in design
- Manufacturing robustness with respect to design, and design relevance of process optimization and control.

A bidirectional link between design and manufacturing is needed. It is provided through accurate process and device models that are available through TCAD. While real measured data is crucial, the power of TCAD lies in the fact that it can capture and address issues that lie beyond the capabilities of process step control and metrology.

For example, TCAD can capture the effects of small temperature variations. TCAD can also capture the atomistic process variability that leads to dopant fluctuations in the channel of minimum width transistors and consequently to large variations in threshold voltage. This is important in the design of SRAMs.

TCAD simulations indicate that a transition from planar transistors to 3D multigate devices such FinFETs may be needed to meet performance targets, but show that this will in turn require changes in the layout of cell as well as new device extraction techniques. Extensive simulations with calibrated TCAD allow the user to capture the relationships between individual process parameters and key device characteristics and cast them into efficient and fast mathematical models called Process Compact Models (PCM). The PCMs provide robust ways of transferring the process and device information into manufacturing, to monitor and control the manufacturing process in manufacturing execution and yield management.

Versions of PCM that link process parameters with Spice parameters can be used to create accurate, process-aware netlists from simulations. These in turn allow the effect of different process variations on key cell characteristics such as timing. PCMs therefore allow the translation of process variability data collected in manufacturing into a form useful for designers.

Through TCAD, it is thus possible to extend DFM and DFY beyond printability issues towards complete process and device architectures and their inherent variability, and to provide the required bidirectional link between design and manufacturing.

The impact on design

Let us focus back on the issues of design. Currently, the design for a new technology node begins almost in parallel with process technology development. Custom and standard cells are developed using design rules and Spice models based on a silicon data complemented by TCAD simulations.

For 65nm and beyond, standard design rules and conventional physical verification may not be sufficient to ensure yield without severe penalties to cell density. A combination of different simulation tools is needed to optimize cells for yield and to make them robust to the process variations expected in manufacturing. Lithography simulations over the entire lithography process window can identify patterning hot spots in the cell that can cause hard defects such as open and shorts.

From a design point of view, however, the interest lies in performance constraints such as power and timing as well as reliability. Lithography optimization can be paired with TCAD to ensure that a combination of worst-case lithography and other process steps does not lead to failing circuits.

The proposed new design flow that captures above requirements is shown in Figure 2. TCAD-derived PCMs, described earlier, can be be combined with the capabilities of physical verification tools to identify potential performance hot spots such as leaky or slow devices.

An example is presented in Figure 3, which shows a standard cell at the 65nm node. The gate layer has undergone OPC to ensure proper line width control. The image is simulated at a defocus of 200nm. The final poly shape exhibits variations in gate length

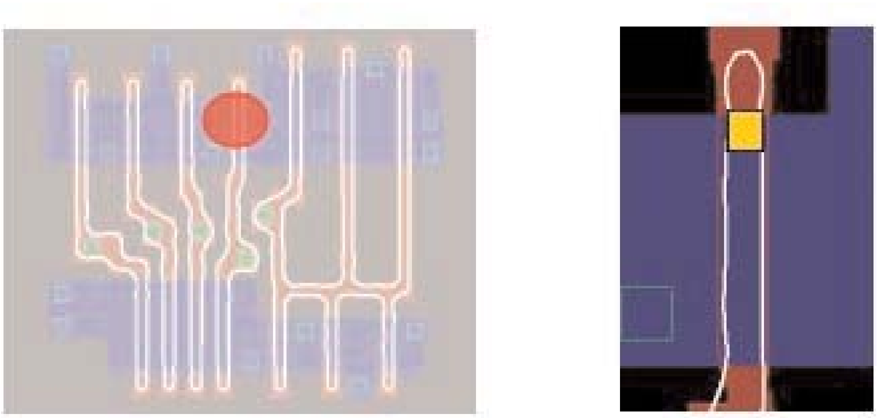

Figure 3 — Lithography simulation of a 65nm standard cell that has undergone OPC indicates necking of a specific transistor gate at a particular location. This is not an open, but electrical verification of the specific region of the gate using TCAD-based PCMs indicates a potential leakage problem.

along the width of several of the transistor gates.

Based on TCAD results, these process-induced geometrical variations can be expressed by an effective gate length for the individual transistors. TCAD simulations might even indicate that under certain process conditions, one of the gates will leak at one specific location. Fine-tuning the OPC rules or slightly modifying the design layout can avoid the problem.

We take a similar approach to other lithographic layers, especially in the back end of the process. For example, we perform parasitic extraction on the "printed" layers that include the effects of pattern definition and transfer.

Summary and outlook

To summarize, for true DFM and DFY it is necessary to look beyond printability issues and address process variability. Manufac-turability issues also need a closer union of design and manufacturing and mutual awareness. TCAD is key to linking both sides. The resulting bidirectional flow of data will change approaches and methodologies on both sides.

Compared to a conventional flow, the advantages of our new design methodology are obvious. Simulated-based, calibrated device models are tightly linked to the underlying manufacturing process and its inherent variations. Utilizing these models in the design flow leads to more realistic cell descriptions. For the first time, this concept makes it possible to directly include the impact of process steps and their inherent variations on the performance of a cell — the ultimate DFY methodology.

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