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Strain Engineering
and Layout Context Variability at 45 nm

We review the various stress sources at the 45 nm node, discuss a methodology for treating the layout dependency, and examine the potential of hybrid-orientation technology (HOT).

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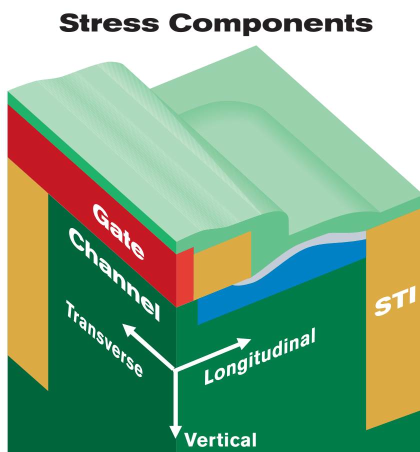
Stress engineering has become a ubiquitous technique for enhancing transistor performance to meet International Technology Roadmap for Semiconductors (ITRS) targets for sub-90 nm CMOS devices. Stress is generated by a variety of sources, such as dual stress liners (DSLs), embedded silicon germanium (eSiGe) in the source and drain (S/D), and stress memorization, as well as unintentional stress from shallow trench isolation (STI). Together, these stresses result in a layout-dependent, non-uniform stress distribution. The layout dependency and anisotropic stress-dependent conductivity in silicon require instance-based annotation of the netlist to account for electrical performance changes to individual transistors.



1. Transverse, longitudinal and vertical stress components in a MOSFET.

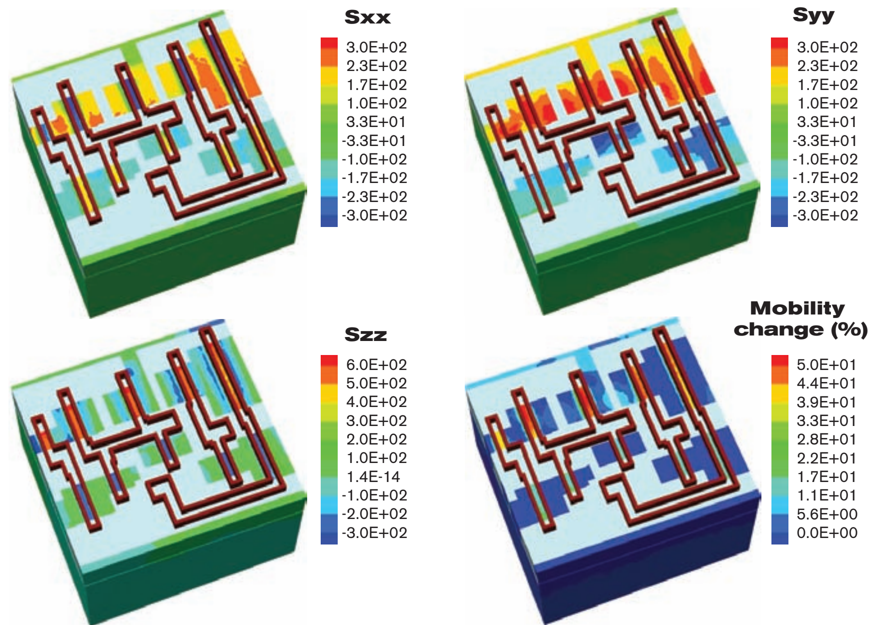
Application of stress engineering
It has long been known that the energy gap and carrier mobility in silicon are modified with mechanical stress, an effect that saw early commercial use in piezoresistive pressure transducers. More recently, the role mechanical stress plays in MOSFET performance has gained great significance because, if properly controlled, it significantly boosts transistor performance in the form of enhanced drive currents caused by improved mobility of carriers (electrons in n-channel transistors, holes in p-channel transistors).

Stress in silicon can be divided into intentional and unintentional stresses. Unintentional stress is a product of normal process steps, such as oxidation, etch, deposition and silicidation, of which the most prominent is the compressive stress resulting from the oxidation used in STI.

Intentional stress is used to engineer stress into the channel of the nFET or pFET (Fig. 1). To enhance n-channel transistors, it is desirable to apply tensile stress in the longitudinal and transverse directions. For p-channel transistors, however, longitudinal compressive stress enhances performance while transverse compressive stress harms performance. Stress liners are used on both the pFET and nFET (DSLs) to transfer tensile or compressive stress to the underlying silicon channel. To introduce compressive stress caused by the lattice constant mismatch between silicon and SiGe, eSiGe is used in pFET S/D regions.

In general, because none of the stress engineering techniques result in purely uniaxial stress, technologists attempt to create stress patterns with one dominant component to approximate the ideal uniaxial case. Still, the combined effect of the various unintentional and intentional stress sources is three-dimensional. Figure 2 shows the three stress components from simulation of a library cell. In particular, the Sxx and Syy components exhibit complex dependencies that motivate mechanical stress simulations at the cell level to characterize the impact on mobility enhancement.

The layout context of strain
The stress distributions shown in Figure 2 depend not only on the process variables used to create the stress sources, but also on the layout. Changes to the volume of STI or SiGe S/D regions alter the stress level in the channel and, therefore, introduce variations in the stress-enhanced performance



2. Stress components from mechanical stress simulation of a library cell. The figure at the bottom right shows the mobility change resulting from this stress field.

across the chip. The systematic variation brought about by the layout-induced stress and mobility changes needs to be accounted for in the design phase because the impact on circuit performance can be sizable.

Recent versions of compact models have introduced a length of diffusion (LOD) model to account for the impact of STI proximity to the channel region. The LOD model modifies the compact model parameters of isolated transistors based on their layout; for instance, the length of the diffusion rectangle and the distance of the gate from the adjoining diffusion edge of either side. However, the LOD model does not account for neighborhood effects, such as adjoining diffusions, or more complicated diffusion patterns.

Similar complexity arises when SiGe is embedded in pFET S/D regions. The volume of SiGe, which sets the level of compressive stress applied to the adjacent silicon, is a function of the poly-to-poly pitch.

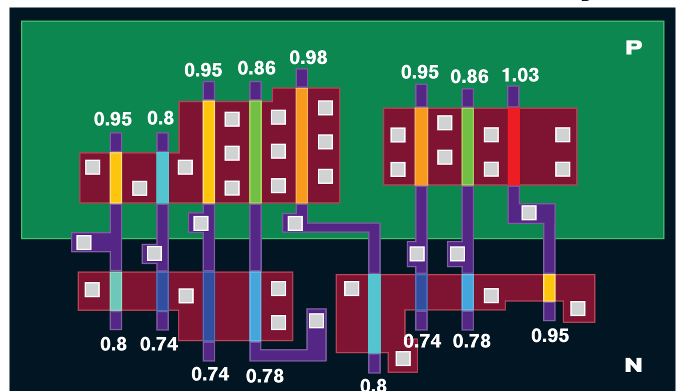
Clearly, designers need more detailed model-based tools to analyze layout stress and compute the changes to the electrical characteristics of transistors. To address this need, we developed a stress analysis tool that efficiently calculates the changes to transistor electrical performance caused by layout-induced stress variability. Figure 3 illustrates the dramatic impact that layout-induced stress variability can have on transistor drive current in a library cell. For each transistor in the cell, the numbers indicate the drive current normalized to the nominal case when the layout context is neglected. In this example, all transistors except one experience performance degradation — namely, as much as a 30% decrease in drive current.

Certainly, many cases will not be as pessimistic as this one, and some will actually produce stress distributions that enhance transistor performance beyond the nominal cases. The conclusion is that model-based tools are needed to account for these effects, because such tools can treat the complex interactions of multiple stress sources with layout parameters.

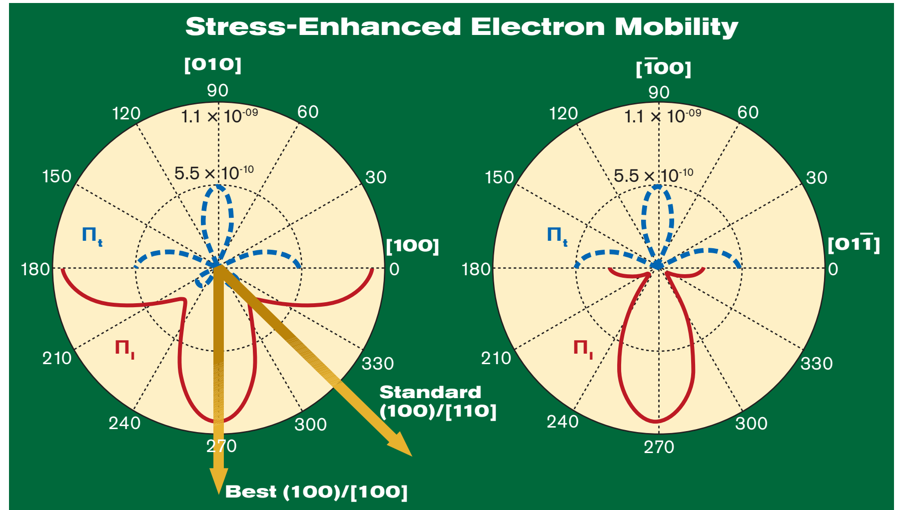
Considering HOT

Until now, the discussion has assumed silicon substrates of (100) surface orientation. This is the norm in today's technology, and is a legacy from the days when the lower density of dangling bonds and interface trap density of the (100) surface relative to other surfaces was a significant technical advantage. However, with decreasing gate dielectric thickness, the impact of interface trap density on threshold voltage (V_t) and subthreshold slope is reduced, opening up the possibility of using other surface orientations with higher stress-induced mobility.

To examine this option, let's look at the anisotropic dependence of the mobility enhancement caused by stress plotted in polar coordinates for a given surface orientation. The polar angle represents the in-plane crystallographic direction along which current is flowing. Figure 4 depicts the relative magnitude of the longitudinal (Π_l) and transverse (Π_t) piezoresistance coefficients for (100) and (110) surface orientations. It is clear that under longitudinal tensile stress, the [100] direction is preferred for both surface orientations.



3. Normalized drive current in a library cell analyzed using the Seismos LX simulator.



4. For maximum electron mobility (pFET), longitudinal tenile stress is preferred on both (100) and (110) surface orientations.

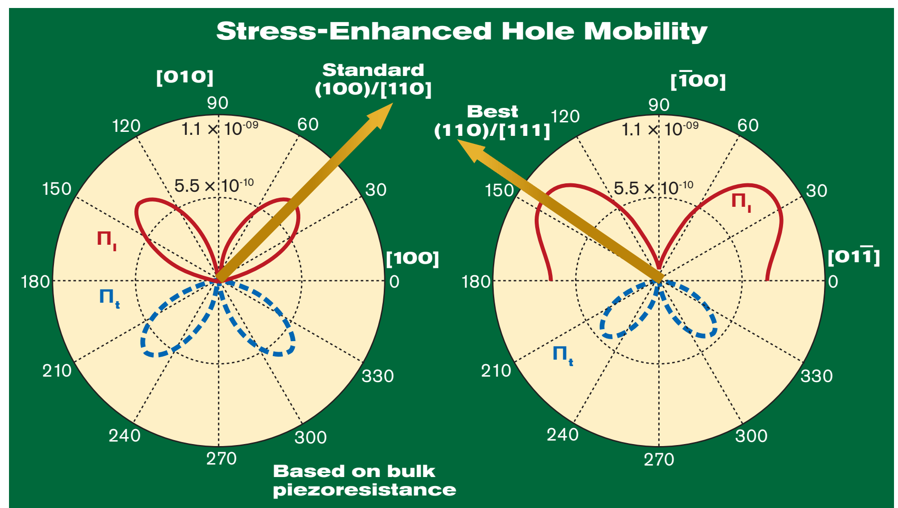
In the case of hole mobility, the highest piezoresistance coefficient is obtained for the [111] direction on the (110) surface under compressive stress (Fig. 5).

This raises the possibility of defining a technology flow whereby the n-channel devices are built on the (100) surface with the channel oriented along the [100] direction, and the p-channel devices are built on the (110) surface with the channel oriented in the [111] direction. This is the essence of hybrid-orientation technology (HOT).

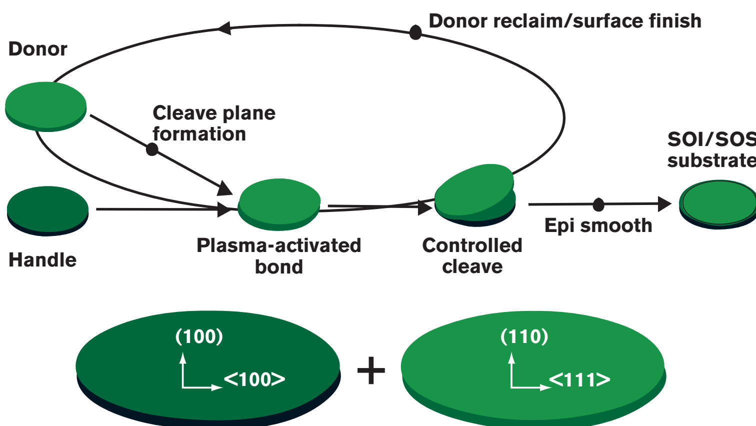
Various techniques proposed to achieve HOT leverage recent advances in wafer-bonding technology. For example, a (110) surface-oriented donor wafer can first be oxidized and implanted with hydrogen to form a region of defects at a well-defined depth (Fig. 6). The donor wafer is then flipped and bonded to a (100) surface-oriented handle wafer. Upon adding thermal energy, a controlled cleave at the location of the hydrogen-induced defects can be performed. The wafer can then be polished using standard chemical mechanical polishing (CMP) techniques to prepare for further processing.

To form the distinct (100) and (110) surfaces, the wafer is patterned and the top layer of silicon is etched down to the underlying silicon (Fig. 7). Through selective epitaxial growth, (100)-oriented silicon fills the etched cavities, resulting in a substrate with silicon islands of (100) and (110) surfaces for fabricating n-channel and p-channel transistors, respectively.

The practical realization of this flow needs to overcome several obstacles left out of the above depiction, including protection of the sidewalls during epitaxial regrowth so that silicon seeds the growth on the bottom. Overall, however, several recent reports indicate that these obstacles are surmountable.



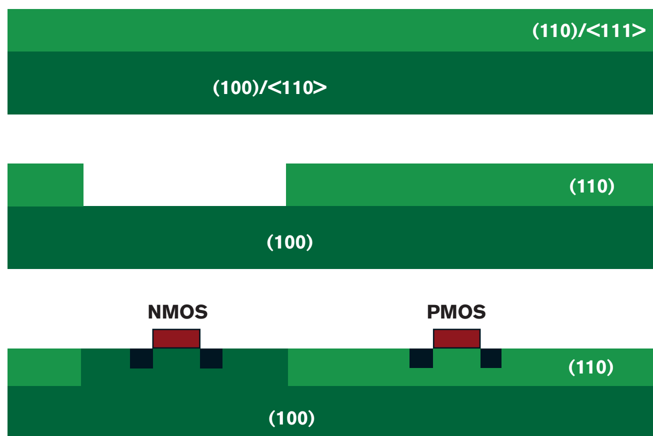
5. The greatest hole mobility (nFET) is obtained for the [111] direction on the (110) surface under compressive stress.



Conclusions

Stress engineering is an indispensable technique for meeting transistor performance targets in sub-90 nm CMOS technology. Multiple stress sources are typically applied to engineer specific levels of tensile and compressive stress to enhance n-channel and p-channel devices, respectively. Yet, stress distributions are three-dimensional and layout-dependent, which creates a need

6. Wafer-bonding can be used to manufacture a substrate with hybrid-orientation.



7. Patterning and epitaxial regrowth in wafer-bonded HOT.

for model-based layout stress analysis tools to properly account for the impact of stress on transistor performance. As further improvements in transistor performance are sought with scaling below the 45 nm node, novel process techniques such as HOT are being investigated as avenues to continue gaining ever-higher performance from silicon CMOS technology. **SI**

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