

## **A New Approach to Higher Yielding Silicon**

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The production of leading edge semiconductors relies on a delicate balance between design and manufacturing. On the manufacturing side, a number of issues conspire to lower yield, degrade performance and increase power consumption. Specifically at 65nm, design sensitivity to lithography, chemical-mechanical polishing and random particle defects can significantly lower initial yield and impose a delay in yield ramp. Yet designers are faced with ever more complex design specifications and tightening tapeout schedules. How can these two domains be bridged to realize higher yielding designs while still meeting aggressive schedules?

### The Three Critical Yield Loss Mechanisms at 65nm

Until recently, yield loss was a problem handled primarily on the manufacturing side. Designs were created based on a set of design rules, and if the rules were obeyed, the design had a reasonable chance to yield well. This began to change as the lithography process failed to keep pace with the rest of the semiconductor process. Yield was further jeopardized when a major material shift occurred and copper was used in a large number of designs beginning at the 130nm node. Of course random particle defects have always played a part in manufacturing yield. Today, as designers struggle to create designs at the 65nm technology node, lithographic sensitivity, poor surface planarity and sensitivity to random particle defects have emerged as the three critical yield loss mechanisms.

Semiconductor manufacturers have become adept at dealing with these challenges and have incorporated tools and technologies to help compensate for an increasing variety of yield loss mechanisms. But these issues cannot be treated in isolation; manufacturing must work more closely with design to enable higher yielding silicon. By leveraging information already existing within the manufacturing domain, semiconductor companies can drive this critical data upstream into the design space and enable DFM tools. This notion is especially powerful in cases where tools using the same core technology are deployed in both manufacturing and design.

### Yield loss due to lithographic sensitivities

The challenge of accurately patterning a design layout onto a wafer has never been greater. This is due to the delayed development and deployment of advanced lithography equipment needed to print the microscopic features of a 65nm chip. The current generation of 193nm lithography equipment is now being extended for service at the 65nm and 45nm technology nodes. This combination of nanometer technology node and lithography equipment with only a fraction of the necessary resolution results in extremely poor printability. In the absence of higher resolution equipment, various resolution enhancement technologies (RET) have been introduced and widely adopted to increase design printability. Even with these technologies, design patterns often experience distortions at some process conditions, changing the electrical behavior of the circuit. In severe cases, a pinch causing an open circuit a metal or poly line, or a bridge causing a short circuit between two lines, can destroy the functionality of the circuit. In other cases, the lithographic effects described above affect transistor leakage and switching delay, metal capacitance and timing, causing degraded circuit performance and power consumption. The result is greater variability leading to parametric yield loss.

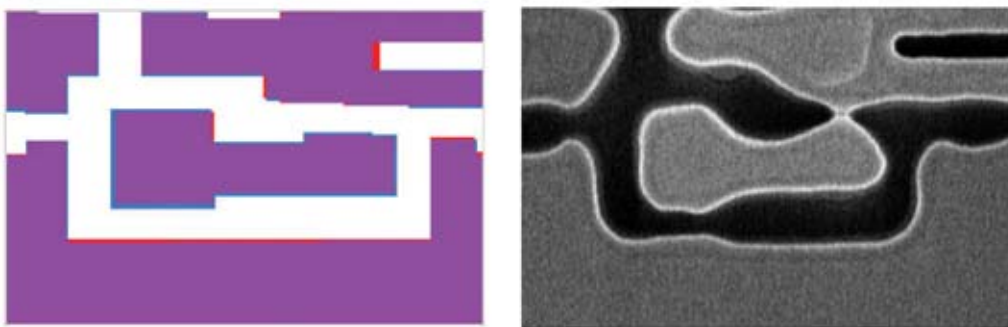
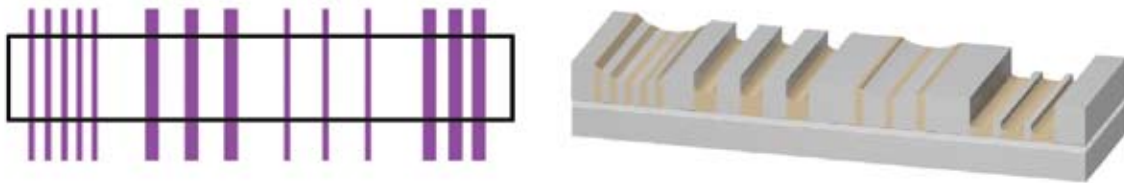


Figure 1: Layout and SEM view for same structure, illustrating a pinch condition in an area where design rules were met.

### Yield loss due to poor wafer planarization

At the 130nm process node, a major shift occurred when many semiconductor companies switched from aluminum to copper as their metal interconnect of choice. In the aluminum process used for previous process nodes, metal is deposited and then etched to create the interconnect lines. An additional deposition of inter-layer dielectric (ILD) is used to isolate the interconnect lines, followed by a planarization step. The flow is quite different in the copper process. For copper, the pattern for the metal traces is etched into the ILD and copper is electroplated into the newly created trenches. The excess copper material is removed in a chemical-mechanical polishing step. As a result of this process, variations in wafer height may appear in areas where the metal density is not uniform. Areas where wide metal lines exist can experience erosion, a condition where too much copper material is removed. In locations where the space between metal lines is smaller, dielectric dishing can occur. The result is greater electrical variation and aggravated depth of focus issues due to varying wafer surface height.



**Figure 2: Top-down and cross sectional representation illustrating the effects of CMP on metal patterns of varying width and spacing.**

Like the lithographic effects mentioned earlier, the variations resulting from poor planarization result in additional parametric yield loss. These variations manifest themselves as increased variability in timing due to the increased resistance in the interconnects. Excess timing variations may affect the ultimate operating frequency of the chip, or may cause internal timing violations which can destroy the functionality of the chip.

### Yield loss due to random particle defects

As mentioned above, yield loss due to random particle defects has been understood for many process generations. During semiconductor processing, random particles can attach to the wafer surface and cause an unintended short circuit between two design elements, creating a bridge fault and destroying the function of the chip. In the same manner, a defect can also sever a physical net in the circuit, preventing the device from functioning correctly by creating an open circuit condition. The random defect-limited yield can be described with the Poisson equation, where CA is the critical area for the design and DD is the defect density inherent in the process:

$$Y = e^{-(CA*DD)}$$

When either CA or DD increase, the probability of a good device decreases, lowering yield. The designer owns the critical area; the foundry owns the defect density. The designer can increase yield by lowering the critical area for the design. This simply means reducing the areas of the design that can be negatively impacted by a random particle defect.

### Creating High Yielding Designs

Now that the three most important factors impacting yield at 65nm are understood, what can be done? Tools which can analyze a design for these three concerns are necessary as a starting point. But more importantly, these analysis tools must link tightly back to the design flow and support the implementation of design changes to enhance yield. At the same time, these yield fixes must be applied in a way that does not create a new yield issue in another domain. Also, these changes must be implemented without adversely affecting timing, power, signal integrity and other critical design metrics.

### Correcting for yield loss due to lithographic sensitivities

Lithographic sensitivities in the design are discovered by applying a process simulation to the design layout and examining the results for potential pinches, bridges, CD variation and areas where contacts or vias can become uncovered. The most accurate simulation techniques exactly match the golden mask synthesis flow, ensuring that each step in the RET process will be faithfully reproduced and the final simulated results will accurately match those used in the actual production process. Utmost accuracy is required to avoid generating “false positives” or layout locations where a hotspot is predicted but does not exist. More importantly, an accurate simulation is more likely to catch every potential hotspot and flag it for correction.

Once a hotspot is identified, it must be corrected to prevent a catastrophic design failure or to reduce excess variation and increase parametric yield. One option is to manually correct the layout by moving polygons in a layout editor. Unfortunately, because of the complex RET used to print 65nm designs, the correction for a given situation is not always intuitive. In addition, there may be hundreds of potential hotspots needing attention, far too many to be corrected productively by hand. In the case of interconnect correction, a close cooperation between the analysis tool and the routing tool is required to intelligently correct potential hotspots in a reasonable time within the normal router flow. Working in the background, the analysis tool determines if a hotspot condition exists on the routed layers. Working in the background, the analysis tool determines if a hotspot condition exists on the routed layers, feeding correction guidance to the router when a hotspot is found. This find – prioritize – fix methodology occurs seamlessly within the normal router flow, coupling real time analysis and correction to create higher yielding silicon.

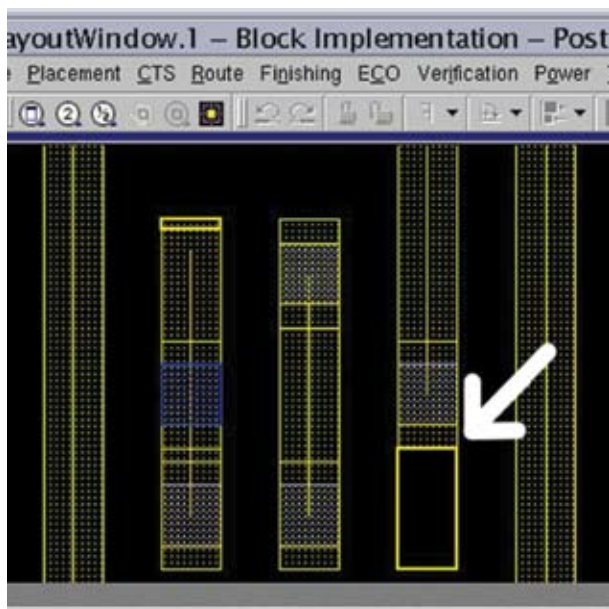


Figure 3: Design layout after hotspot analysis, illustrating automatic correction guidance applied by router.

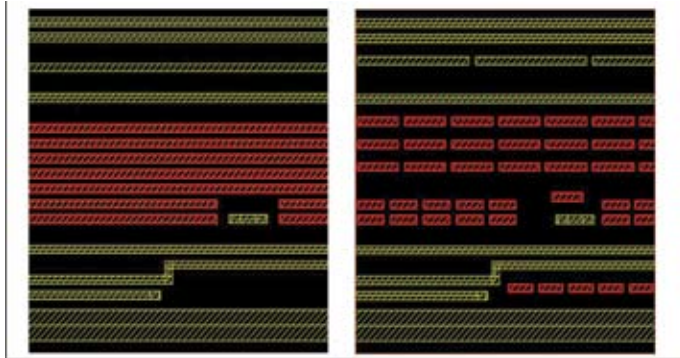
### Correcting for yield loss due to poor wafer planarization

As described previously, non-uniform metal distribution can cause uneven wafer surface height, in turn causing excess variation in signal timing and parametric yield loss. An analysis performed on the design layout can determine if it may suffer from poor planarization. The design is first partitioned into small squares. Next, the layout areas defined by each square are analyzed and parameters such as metal density and perimeter are extracted. Using the extracted data, the wafer surface height for each region is modeled. Finally, a wafer surface profile is created to identify areas of excess surface height variation. By analyzing a heat map representing the die surface, engineers can quickly determine where problem areas exist.

To correct for planarity issues, rule-based metal fill is a common approach for inserting dummy metal fill to achieve uniform metal distribution and adequate planarization. A DRC tool is used to apply the fill, driven by a set of CMP design rules to constrain the fill algorithm. More complex fill strategies may incorporate a library of fill patterns with different sizes and shapes. Simple fill algorithms may apply the metal insertion in a single pass; more complicated algorithms begin with larger patterns and apply smaller and smaller pat-

terns in subsequent passes. A fundamental limitation exists in with this technique: timing impact, especially on timing-critical nets, is not considered. As a result, the metal fill may aid wafer planarity at the expense of circuit timing.

Rather than introduce an additional correction step which may compromise the timing of the circuit, the best approach is to employ correction within the normal router flow. The analysis tool works seamlessly in the background, advising the router on an optimal fill strategy while the router performs timing-driven metal fill. The analysis tool can also be used in a stand-alone manner to separately validate the design for the existence of planarity issues. Using this approach safeguards design timing while creating a design with the best possible planarity.

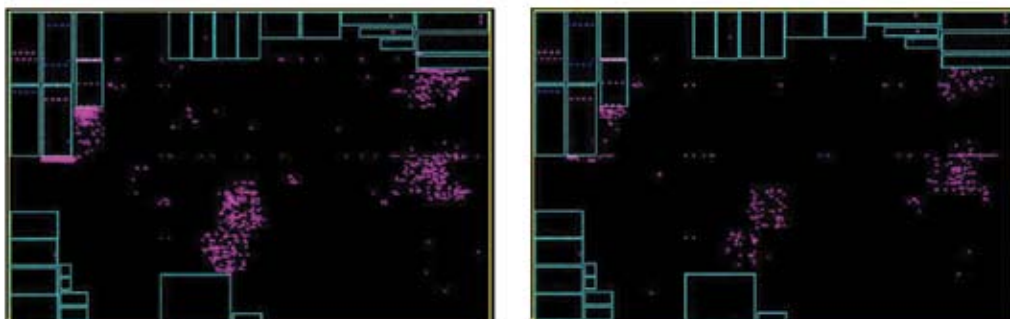


**Figure 4: Metal fill, shown in red, is applied to same layout using a rule-based approach (left) and a model-based approach (right). The model-based approach provides much better uniformity.**

### Correcting for yield loss due to random particle defects

Random particle defects can destroy circuit function by creating an unintended bridge or break condition in the layout pattern. A critical area analysis is performed on the design to predict the possibility of these manufacturing faults. This analysis determines a particular layout's sensitivity to random particle defects, given different defect sizes likely to be found in the process. Using the critical area information together with the defect density data for the different defect sizes, the predicted yield loss due to random particle defects can be calculated.

But how can these issues be reasonably corrected in a design? The most common ways to reduce critical area is to make the interconnect lines wider and create additional space between the circuit lines. This must be done in a way that does not increase the area for the whole chip and facilitates spreading and widening of the wires into the open areas of the design. If space allows, via redundancy should also be incorporated by creating double vias wherever possible.



**Figure 5: Layout view illustrating critical area before (left) and after (right) wire spreading and widening. Note the significant decrease in critical area on the right.**

Again, the routing tool is best place to perform this critical yield optimization step. The router understands the impact of wire spreading, wire widening and via doubling on timing and other domains, and can perform critical area-based yield optimization while maintaining timing and area integrity.

### **Summary**

This paper has discussed the three most important yield loss mechanisms in 65nm designs, and proposed methods for mitigating yield loss without severe impact to design schedules. Using tools that are both powerful and well-integrated, design and layout engineers can create high yielding designs while meeting design specifications and demanding schedules.

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