

# PrimeTime

## Golden Timing Signoff Solution and Environment

### Overview

Signoff users generally have four key solution requirements in order to meet their design requirement needs: continuous improvement to runtime and capacity to address increasing chip size requirements, efficient multi-scenario analysis to verify timing across all corners and modes, margin control to reduce over-design and maximize chip performance, and accuracy to insure correlation to silicon. The Synopsys PrimeTime® Suite addresses these requirements by delivering fast, memory-efficient scalar and multicore computing, distributed multi-scenario analysis and ECO fixing, using advanced constraint analysis, and variation-aware Composite Current Source (CCS) modeling that extends static timing analysis to include Crosstalk Timing, Noise, Power and statistical STA.

### PrimeTime Suite

The Synopsys PrimeTime suite, including PrimeTime, PrimeTime SI, PrimeTime VX and PrimeTime PX, provides a single, golden, trusted signoff solution for timing, signal integrity, power and variation-aware analysis. It delivers HSPICE® accurate signoff analysis that helps pinpoint problems prior to tapeout thereby reducing risk, ensuring design integrity, and lowering the cost of design. This industry gold-standard improves your team’s productivity by delivering fast turnaround to shave precious time from development schedules for large and small designs while ensuring first-pass silicon success through greater predictability and the highest accuracy.

### Benefits

#### HSPICE-Accurate Results Minimize Over-Design

HSPICE-accurate analysis pinpoints timing problems quickly and reduces ECO fixing time. Use of CCS models provides consistent results for static timing, signal integrity, power, and variation-aware analysis. Path-based analysis is available to zero-in on your most challenging timing paths. Advanced on-chip variation modeling and variation-aware analysis deliver additional margin control. This helps designers avoid the over- and under-design of chips reducing overall costs and shaving valuable time from design schedules.

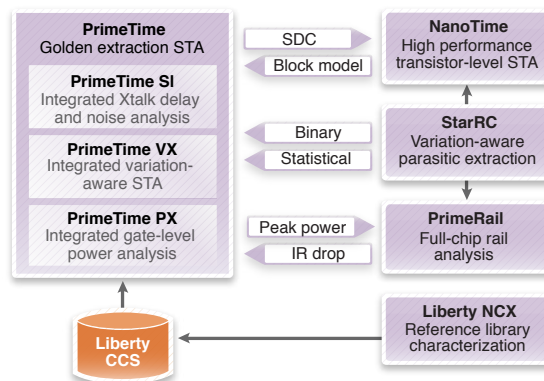


Figure 1. Galaxy signoff solutions

## ***Integrated Design Environment Improves Productivity***

The unified analysis environment in the PrimeTime Suite enables designers to perform complete timing, signal integrity, power and variation-aware analysis in a single environment which improves designer productivity, reduces set-up steps, as well as minimizes the number of interface files created and used. This leads to faster time-to-results because identical operations, such as timing and slew calculations, are not repeated. Costs are minimized by eliminating the need for multiple products with associated support costs.

## ***Fast Turn-around Time Speeds Analysis and Signoff***

PrimeTime offers a range of solutions to reduce time required for analysis and signoff. Distributed Multi-Scenario Analysis (DMSA) enables multiple scenarios to be run concurrently which reduces wall clock time and produces a single comprehensive timing report. Coupled with features such as automated hold-fixing that reduce ECO time from days to minutes, this capability reduces timing closure turn-around time and improves engineering productivity. New multicore support further reduces the time required for static timing and signal integrity analysis.

## ***High Capacity Approach Reduces Hardware Costs***

Using multiple cores across existing machines is one of the many ways PrimeTime reduces the size (and cost) of the hardware required for timing signoff and analysis to analyze engineer's largest designs. Other techniques include intelligent disk-caching for reduced memory footprints and multi-threading for faster performance.

## ***Complete Solution Ensures Comprehensive Signoff***

Comprehensive timing and design rule checking, extensive design constraint annotation and delay reporting allow ASIC and COT designers to signoff with

confidence knowing that all aspects of their designs have been analyzed.

## **PrimeTime**

The Synopsys PrimeTime static timing analysis solution is the most trusted and advanced timing signoff solution for gate-level designs. It is the industry's de-facto gold standard for gate-level static timing analysis with the capacity and performance for 100+ million instance chips being designed at 40-nm and below. PrimeTime static timing analysis and StarRC™ parasitic extraction are industry gold standards, and key components of the Galaxy™ Design Platform.

The PrimeTime STA solution provides a comprehensive and unmatched environment for timing signoff and timing analysis. It provides to designers extensive timing analysis checks, advanced on-chip variation analysis techniques, golden delay calculation, advanced modeling, unmatched productivity and ease-of-use, a graphical user interface, and industry-wide ASIC vendor signoff and foundry support.

The PrimeTime static timing analysis solution provides the foundation and environment for a suite of extensions in signoff analysis. In addition to timing analysis, PrimeTime SI, PrimeTime PX, and PrimeTime VX deliver extensions for signal integrity analysis, leakage and dynamic power analysis, and variation-aware analysis.

## ***Comprehensive Timing Analysis***

PrimeTime has an unparalleled number of timing analysis capabilities to enable signoff of the most complex designs. The comprehensive set of timing and design rule checks combined with extensive design constraint annotation and delay reporting, allow designers to peer into all aspects of their designs, and confidently analyze and signoff their design.

```
read_verilog mpeg.v
current_design mpeg
link
read_parasitics ....
create_clock -period 10.0 clock
...
...
report_timing
```

Figure 2: Standard PrimeTime flow

## ***Golden Delay Calculator***

PrimeTime's built-in RC delay calculator uses parasitic information and Composite Current Source (CCS) libraries to calculate cell and interconnect delays with SPICE-like accuracy. The extensive delay calculation and parasitic annotation reporting capabilities enable designers to easily debug and pinpoint problems thereby improving productivity. The advanced delay calculator supports voltage and temperature scaling between libraries. This enables multi-voltage analysis and eliminates the need to maintain a large collection of libraries for each unique process-voltage-temperature (PVT) point.

## ***Advanced On-Chip Variation (AOVCV) Analysis***

At 65-nm and below, the traditional approach of using a global derate margin to account for on-chip variations (OCV) can add excessive margins and result in over-design, reduced design performance, and longer design cycles. PrimeTime's advanced on-chip variation (Advanced OCV) modeling capability extends OCV analysis to deliver an improved method of adding margin in a design. Advanced OCV uses context-specific derate factors that consider location and logic depth of each path being analyzed. As a result, excessive design margins are reduced and fewer timing violations are seen. The pessimism-reducing approach of Advanced OCV reduces over-design and enables designers to reach timing closure quicker and with greater confidence.

## Distributed Multi-Scenario

### Analysis (DMSA)

The greater design functionality and complexity afforded by today's smaller geometries combined with accompanying physical phenomena has led to an explosion in the number of scenarios which need to be verified. Verification of a chip design requires analysis of many individual scenarios that represent different operational modes and voltage, temperature and process corners. Analyzing and managing the analysis of these scenarios is simplified with PrimeTime's Distributed Multi-Scenario Analysis (DMSA) capability. DMSA allows designers to set up, distribute, run, and perform ECO fixing simultaneously across multiple scenarios, thereby reducing overall turnaround time.

## Additional Features in PrimeTime

- ▶ Advanced modeling capabilities with Interface Logic Models (ILM) and Extracted Timing Models (ETM)
- ▶ UPF (Unified Power Format) support
- ▶ Graphical User Interface (GUI) enabling timing analysis and design visualization using schematics, histograms, tables, and tree graphs
- ▶ Save and restore
- ▶ What-if ECO analysis
- ▶ Exception and constraint analysis for debugging
- ▶ ASIC vendor signoff and foundry support
- ▶ Extensive support of industry-standard input and output
- ▶ file formats

```
set si_enable_analysis TRUE
read_verilog mpeg.v
current_design mpeg
link
read_parasitics -keep_capacitive_coupling
create_clock -period 10.0 clock
...
report_timing -crosstalk_delta
report_noise
```

Figure 3: PrimeTime SI flow  
— Easy to use and adopt

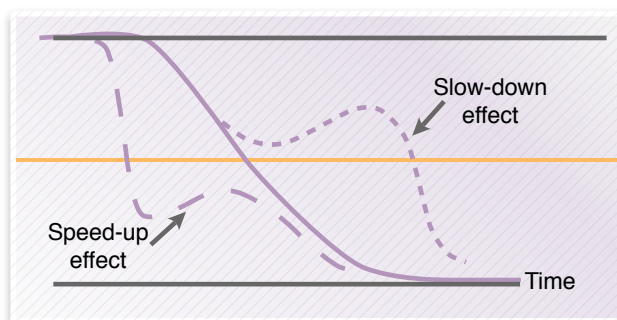
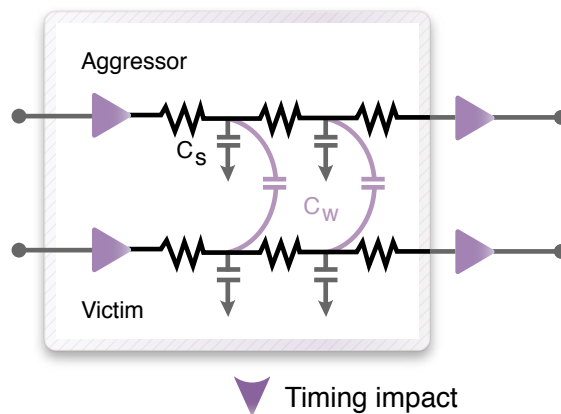


Figure 4: Crosstalk delay analysis pinpoints crosstalk timing failures.

## PrimeTime SI

With shrinking process geometries and rising clock frequencies for nanometer designs, signal integrity (SI) effects such as crosstalk delay and noise (or glitch) propagation can cause functional failures or failed timing. It is essential for designers to address these SI problems to ensure that their designs are delivered to market correctly in the shortest amount of time. Time-to-market pressure, chip complexity, and control of SI effects are all factors requiring an accurate, fast, and trusted analysis and signoff solution.

The PrimeTime SI solution extends the trusted, tape-out proven PrimeTime static timing analysis and signoff environment by adding accurate crosstalk delay, noise (glitch), and voltage (IR) drop delay analysis to address signal integrity effects at 90-nm and below.

### Ease-of-Adoption and Use

PrimeTime SI, an extension of PrimeTime Static Timing Analysis (STA), is easy-to-use and adopt. It utilizes the familiar PrimeTime flow and environment, with common commands, user interface, reports, and attributes. (See figure 3)

## Comprehensive SI Analysis Built into the PrimeTime Environment

The unified approach of signal integrity and timing analysis delivers a comprehensive and time-efficient method to concurrently analyze noise and crosstalk delay effects on timing. Additionally, the concurrent analysis in a single tool enables faster results while improving designer productivity.

### Accurate Crosstalk Delay, Noise (glitch) and IR Drop Analysis

Signal integrity effects are interdependent and need to be analyzed in the context of timing. PrimeTime SI uses an integrated golden delay calculation engine with the proven and trusted PrimeTime static timing analysis engine to accurately model and compute timing deviations due to crosstalk and IR drop. PrimeTime SI has the capacity and performance required to perform accurate noise calculation, detection, and propagation on the largest of today's designs. (See figure 4)

## Additional Features in PrimeTime SI

- ▶ Reduces false violations by considering slew propagation, timing

windows, and logical correlation of signals

- ▶ Hierarchical SI analysis capabilities using ILMs with crosstalk
- ▶ Adaptive waveform propagation
- ▶ Multi-voltage support
- ▶ SPICE deck output
- ▶ Includes fast CCS noise library characterization utility

## PrimeTime VX

The PrimeTime VX solution extends the PrimeTime environment to analyze device and interconnect variations at 65-nm and below using statistical techniques. Variation-aware analysis with the PrimeTime VX solution delivers improved margin control, avoiding the over- and under-design of circuits. Design robustness is improved by pinpointing areas of the chip most susceptible to variations so that designers can reduce this sensitivity and improve the parametric yield of production chips. PrimeTime VX analyzes systematic or deterministic process variation (die-to-die) as well as random process variation (on-die) in a flexible environment with a large range of features that can easily be introduced into existing design flows. PrimeTime VX allows users to leverage their existing investment in their trusted PrimeTime STA tool infrastructure, flow and knowledge.

### **High Accuracy, Sample-Based Statistical Timing Analysis**

PrimeTime VX employs a unique approach to statistical timing analysis that delivers very high accuracy without compromising runtime. The PrimeTime VX statistical engine is a Monte Carlo style sample-based engine that delivers signoff accuracy.

This approach ensures that all process parameters, regardless of their distributions and cross-correlations can be accurately modeled in the analysis. Using this approach, PrimeTime VX is liberated from the complex statistical mathematical challenges which are often used by other tools and that can often impact accuracy.

### **Comprehensive, Full Chip Statistical Analysis Solution**

PrimeTime VX delivers full-chip performance and capacity with the comprehensive set of capabilities necessary for signoff. PrimeTime VX adds statistical timing analysis to graph-based and path-based analysis while retaining key capabilities such as Signal Integrity (SI) analysis, clock re-convergence pessimism removal (CRPR), what-if-analysis, bottleneck analysis, IR Drop annotation and distributed multi-scenario analysis (DMSA).

### **Strong Ecosystem**

PrimeTime VX is a part of a complete variation-aware analysis solution provided by Synopsys that includes StarRC VX for statistical RC extraction and Liberty™ NCX for statistical library characterization and quality assurance. Along with our top rated world-wide applications support personnel, trusted library vendor IP, and foundry qualification and reference flows from leading foundries including TSMC and STARC, we have put together a strong ecosystem to ensure design success.

### **Additional Features in PrimeTime VX**

- ▶ Advanced Analysis
  - Integrated corner-based SI
  - VA-timing adjusted bounding SI
  - IR drop annotation
  - Variation-aware constraints
- ▶ Variation Specification
  - Device and interconnect
  - Concurrent Inter-die, intra-die, intra-cell
  - Full, no, auto, cross, spatial, and topological (CRPR) correlation
- ▶ Variation/Sensitivity reports
  - Paths
  - Lib\_cells
  - Cells (graph)
  - Additional Interconnect Variation Parameters
  - Dielectric constant variation
  - Metal & poly resistivity variation
  - Via resistance variation

## PrimeTime PX

The PrimeTime PX solution expands the PrimeTime timing and signal integrity environment to deliver highly accurate dynamic and leakage power analysis for design geometries at 90-nm and below. Designers have a single, unified analysis environment for timing, signal integrity and power analysis that is anchored by the golden PrimeTime static timing solution and delivers the highest productivity and a predictable path to silicon for their most complex designs.

By combining timing, signal integrity and power analysis into a single tool and environment, common operations are not repeated. For example, netlist, parasitic and constraint file reads, and tool setup steps are not repeated. As a result, the PrimeTime PX solution delivers up to two times (2x) faster time-to-results (TTR) over separate, standalone solutions. As an integral part of the PrimeTime environment, power analysis can be performed using common PrimeTime commands, reports, attributes and debugging features. (See figure 5)

### **Full-Chip Timing, SI and Power Analysis**

The unified analysis environment enables designers to perform accurate leakage and dynamic power analysis along with timing and SI analysis. Power and timing analysis are integrated in a single tool, which improves designer productivity by providing results faster with fewer set-up steps. Designers can understand the trade-offs and effects of leakage and dynamic power in the context of complete timing, signal integrity and power analysis by adopting the new easy-to-use methodology from PrimeTime PX.

```
set si_enable_analysis TRUE
set power_enable_analysis TRUE
read_verilog mpeg.v
...
read_parasitics -keep_capacitive_coupling
read_vcd activity.vcd
create_clock -period 10.0 clock
...
report_timing -crosstalk_delta
report_noise
report_power
```

Figure 5: PrimeTime PX flow

### Vector-Free Dynamic Power Analysis

Vector-free dynamic power analysis allows power analysis to be performed without waiting for switching data from simulation. By using the PrimeTime tool's accurate timing windows, vector-free analysis enables precise power analysis early in the design flow to identify blocks with the highest power consumption sooner.

### Statistical Leakage Power Analysis

Statistical leakage power analysis in PrimeTime PX extends PrimeTime suite's statistical technology to leakage variation analysis for advanced designs at 65-nm and below. Variation-aware leakage power analysis in PrimeTime PX reduces the leakage signoff pessimism associated with using multiple process corner libraries. An intuitive, easy-to-use graphical user interface enables designers to make efficient yield versus leakage tradeoff decisions for their most complex power-sensitive designs.

## Additional Features in PrimeTime PX

- ▶ Event-based dynamic power analysis using VCD or SAIF
- ▶ RTL and gate-level VCD and SAIF support
- ▶ Instantaneous and cycle-accurate peak power analysis
- ▶ Average power analysis
- ▶ State-dependent leakage power analysis
- ▶ Analysis of advanced low power design techniques: multi-voltage, coarse-grain MTCMOS
- ▶ Clock tree power estimation
- ▶ Power analysis driver GUI window
- ▶ Distributed Peak Power Analysis
- ▶ UPF support
- ▶ Supports industry-standard NLPM and CCS Power libraries

## Galaxy Signoff Modeling and Platform Support

### Advanced Modeling

The PrimeTime Suite provides a wide range of advanced modeling support. Interface Logic Models (ILM) are provided for hierarchical static timing analysis and signoff. Extracted Timing Models (ETM) are provided, in .lib format, for cell-based reusable IP and physical design flows. Quick Timing Models (QTM) are available for top-down design. A complete set of validation, debugging and model merging features are also provided.

### Platform Support

The following platforms are supported: AMD64, Sparc64, Linux32 4.0, SUSE 32 and SUSE 64

## About Galaxy Design Platform

The Galaxy Design Platform is an open, integrated design implementation platform with best-in-class tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor design tools and the open Milkyway™ database, the Galaxy Design Platform incorporates consistent timing, SI analysis, common libraries, delay calculation, constraints, testability and physical verification to provide a convergent flow from RTL all the way to silicon. The Galaxy Design Platform helps reduce design time, decrease integration costs and minimize the risks inherent in advance, complex semiconductor design.