Overview
StarRC™ is the EDA industry’s gold standard for parasitic extraction. A key component of Synopsys Galaxy™ Implementation Platform, it provides a silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed-signal (AMS) and memory IC designs. StarRC offers modeling of advanced physical effects needed for leading-edge process technologies, including 20-nm, 14-nm and beyond. Its seamless integration with industry standard digital and custom implementation systems, timing, signal integrity, power, physical verification and circuit simulation flows delivers unmatched ease-of-use and productivity to speed design closure and signoff verification.

StarRC Solution
Semiconductor process technology has been continually scaling down for the past four decades and the trend continues. Shrinking process geometries, combined with the use of new device structures and an increasing number of metal layers at each new process node, are introducing millions of new parasitic effects in designs. In addition, soaring design sizes and complexities are increasing the sensitivity of circuits to parasitics due to the increasing impact on signal timing, noise and power. To ensure a successful silicon design and meet tape-out schedules, IC designers need an advanced parasitic extraction solution that delivers signoff accuracy and increased designer productivity. Furthermore, they need a solution that is versatile enough to manage the full design spectrum from custom digital/AMS to full-chip memory and SoC designs.

Synopsys’ StarRC is the next-generation high-accuracy and high-performance parasitic extraction solution for digital and custom IC implementation and signoff verification (see Figure 1). Trusted by hundreds of semiconductor companies and proven in thousands of production designs, StarRC provides sub-femtoFarad-accurate technology for design at advanced process technologies. It achieves its high accuracy by performing detailed modeling of device and interconnect parasitic effects in nanometer process technologies. The advanced modeling and accuracy is complemented with the embedded Rapid3D technology for circuits that require even higher field solver accuracy.

StarRC delivers industry-leading performance and capacity for customers’ gate-level and transistor-level extraction needs. StarRC’s multicore distributed processing technology delivers excellent scalability for efficient utilization of available hardware, and its simultaneous multi-corner extraction feature allows today’s increasing number of extraction corners required for analysis to be processed within a single run with a significantly reduced runtime. Its seamless integration with Synopsys’ leading IC Compiler physical implementation solution, gold standard PrimeTime® signoff suite, Galaxy Custom Designer™ mixed-signal implementation solution, IC Validator physical verification solution, CustomSim™ circuit simulation and other third-party implementation and signoff tools enables users to significantly accelerate their design implementation and verification.
The StarRC extraction solution is available in three different configurations: StarRC Custom, StarRC, and StarRC Ultra (see Figure 2). StarRC Custom offers extraction for high-accuracy custom AMS/digital design, StarRC offers full-chip gate-level and transistor-level extraction, and StarRC Ultra offers high-end extraction for advanced analysis flows, particularly those required at 20-nm and below.

<table>
<thead>
<tr>
<th>Parasitic Extraction Features</th>
<th>StarRC Custom</th>
<th>StarRC</th>
<th>StarRC Ultra</th>
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<tbody>
<tr>
<td>Multicore processing</td>
<td>✓</td>
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<tr>
<td>Advanced process modeling, including 20-nm and below</td>
<td>✓</td>
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<td>Integrated 3D fast field solver (high accuracy extraction)</td>
<td>✓</td>
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<td>Multi-corner temperature sensitivity extraction</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>CustomSim circuit simulation integration</td>
<td>✓</td>
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<td>Custom layout environment integration</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Hierarchical extraction for large transistor-level designs</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Full-chip transistor-level and gate-level extraction</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Physical implementation interface (Milkyway, LEF/DEF)</td>
<td>✓</td>
<td>✓</td>
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<td>PrimeTime binary interface for productivity</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Metal fill reuse for ECO turnaround-time reduction</td>
<td>✓</td>
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<td>Simultaneous multi-corner (SMC) extraction</td>
<td>✓</td>
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<td>Color-aware double patterning (DPT) solution</td>
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<tr>
<td>FinFET modeling and extraction</td>
<td>✓</td>
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<tr>
<td>3D-IC / Silicon Interposer extraction</td>
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<td>Variation-aware extraction (statistical random process variation)</td>
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Figure 1: StarRC provides a next-generation parasitic extraction solution for gate-level and transistor-level digital and custom IC designs.

Figure 2: StarRC offers flexible product configurations for specific design applications.
Benefits

- Foundry gold standard for extraction accuracy with broadest qualification and adoption
- Leader in 20-nm and below process modeling, including most trusted foundry source for state-of-the-art FinFET modeling
- High performance and capacity for gate and transistor-level extraction, including multi-core and simultaneous multi-corner extraction
- Unified 3D fast field solver for critical net, IP, and custom circuit extraction
- 3D-IC extraction solution for interposer and stacked die technologies
- Integration with PrimeTime timing signoff, IC Compiler physical implementation, IC Validator physical verification, CustomSim circuit simulation, Galaxy Custom Designer and other third party implementation and custom design solutions for increased designer productivity

Advanced Process Modeling

Increasing process variation and new parasitic effects introduced at each new technology node are significantly increasing design challenges. Process technologies at 40nm and 28nm have elevated a variety of physical effects once considered secondary to primary factors affecting circuit behavior, risking performance degradation, silicon failure and lower yields if not accurately modeled. In addition, striking changes in process technology, like double-patterning at 20-nm and FinFET transistor architecture at 14-nm and below, are requiring consideration of a host of completely new and complex effects with even more ramifications on extraction, timing analysis and design robustness. More than ever, the accuracy of parasitic modeling and extraction results is contributing to overall design integrity.

Some typical process modeling capabilities offered by StarRC include variation and litho-aware extraction and chemical-mechanical polishing (CMP)-based thickness variation extraction, as well as modeling of micro-loading effects and low K dielectric damage. For transistor-level circuit modeling, gate-to-contact capacitance, gate-to-diffusion capacitance, and contact etch effects are some of the device parasitics which are accurately modeled by StarRC for increased sign-off integrity, with the additional benefit of being modeled in-context with the layout environment for even higher accuracy.

20nm Color-Aware DPT Modeling

At 20-nm, significant capacitance variation is introduced by double-patterning, a fabrication strategy where metal lines on a single layer are created in two separate masking steps to achieve finer metal pitch. Misalignment between the patterns causes coupling capacitance between adjacent metal lines to increase in one direction and to decrease in another (see Figure 3a). StarRC models these capacitance variations with modified DTP process corners, thus ensuring that their effects are accurately accounted for. StarRC also supports “pre-coloring”, which allows designers to force the routing of specific critical nets to be on the same mask layer to remove this capacitance variation for even higher extraction accuracy. StarRC contains a full and flexible solution for precisely modeling the effects of double-patterning in designs at 20-nm and below.

Figure 3: StarRC’s advanced 20-nm DPT and 14-nm FinFET modeling for signoff accuracy
**FinFET Modeling**

Even more radical changes are introduced by FinFET transistor architecture at 14nm and below. In contrast with planar transistors, FinFETs are able to achieve better control over the source-drain channel because the gate encloses the channel on three sides, resulting in higher mobility, greater drive strength, lower switching currents and lower leakage currents. But this multi-gate non-planar architecture also introduces more complex geometries and many new capacitive elements that must be accurately extracted due to their impact on circuit performance. StarRC uses uniquely detailed FinFET physical profile for 3D modeling of layout-dependent middle-end-of-line (MEOL) parasitic effects (see Figure 3b) for increased accuracy. Due to its advanced modeling solution, StarRC is the extraction tool of choice for foundries and IP developers to model new FinFET parasitic effects and ensure proper characterization of FinFET devices.

**3D-IC Modeling**

StarRC also supports extraction for stacked die and silicon interposer 3D-IC technologies (see figure 4a and 4b). StarRC extracts through-silicon vias (TSV) and substrates, TSV-TSV capacitive coupling, silicon interposers, micro-bump structures, and routing layers on each die. StarRC supports modeling substrates as either floating or grounded. StarRC’s extraction and modeling of through-silicon vias (TSV) and substrates through Synopsys’ Interconnect Technology File (ITF) has been qualified by several major foundries and is found in their 3D-IC reference flows.

![Figure 4.a Silicon Interposer and Stacked Die](image)

![Figure 4.b Through Silicon Via (TSV) Modeling](image)
Multicore Processing
Multicore processor hardware has become common due to the widespread need for higher productivity. A large majority of design jobs are run on compute farms consisting of multicore machines, and IC designers seek design tools that harness the full potential of their hardware network. StarRC’s multicore technology works seamlessly with popular commercial grid computing management software to maximize efficiency across multicore processors, as well as multi-processor compute farms, to take full advantage of available hardware. StarRC offers high performance per CPU core; for example, up to 6x scalability on 8 cores. In addition, StarRC multicore processing consists of easy-to-setup compute resource allocation, automated design partitioning to multiple cores, balanced load sharing, and automatic failure recovery for a superior fault-tolerant server environment.

Simultaneous Multi-Corner Extraction
The increase in process variation and decreasing process geometries found in technology nodes at 40-nm and below have resulted in a growing number of extraction corners requiring analysis. This in turn is having a significant impact on the efficiency of designers. To mitigate the increased TAT caused by this rise in extraction corners, StarRC offers Simultaneous Multi-Corner extraction (SMC), wherein all extraction corners can be analyzed within a single run. Runtime speed-up of 3X is achieved when compared to traditional single-corner extraction runs, without degradation in accuracy. Designers will also see a marked decrease in disk space usage.

Metal Fill Re-Use
Inserting metal fill, or floating metal lines which fill in gaps between routing metal, is an effective strategy for reducing process variation due to non-uniform metal density, but in advanced technology nodes, this metal fill significantly impacts parasitic capacitance. Therefore, a realistic model of metal fill is required in a design when performing extraction and timing analysis in the ECO and sign-off timing closure flows. But re-inserting metal fill after each ECO can greatly increase ECO TAT. StarRC’s Metal Fill Re-Use feature solves this problem by allowing designers to insert metal fill once in a design and then re-use that fill in subsequent ECO extractions. Metal shorts created between ECO routing and the original metal fill are “virtually” trimmed away for the purposes of extraction analysis. Extraction results using StarRC’s Metal Fill Re-Use are very close in accuracy to those obtained when re-inserting the metal fill post ECO, without incurring the re-insertion runtime. StarRC allows designers to significantly decrease their total ECO TAT while maintaining tight correlation between ECO and final sign-off timing results.

PrimeTime Binary Interface
Parasitic netlist size and timing signoff analysis runtime are key concerns for designers of large SoC designs at leading-edge process nodes. The extracted parasitic netlist size of a multi-million-net design can be as large as several gigabytes of memory that can significantly impact the parasitic read and analysis runtimes. StarRC provides a unique and compact binary parasitic format, called SBPF (Synopsys Binary Parasitic Format), with the industry-leading Synopsys PrimeTime timing signoff tool. SBPF binary interchange format captures identical electrical and connectivity data as SPEF, but offers significant benefits in parasitic netlist size (up to 15x) and reduced parasitic read runtime (up to 80%) while preserving PrimeTime signoff accuracy.

High Accuracy Fast Field Solver Extraction
For timing-sensitive circuits such as clock networks, memories, AMS/RF, high-speed digital, standard cells and other IP designs, accuracy is a non-negotiable design criterion. Designers of such critical IP and circuits generally require field-solver-level accuracy as well as fast turnaround time. StarRC offers integrated 3D fast field solver extraction, using Rapid3D technology, for efficient higher-accuracy extraction. Building on the Raphael NXT engine, Rapid3D incorporates the latest advancements in field solver algorithms to deliver the highest performing 3D extraction while providing the same gold standard accuracy. The embedded Rapid3D technology complements StarRC’s primary extraction engine for 3-dimensional self- and coupling-capacitance extraction of critical circuits. Within the single StarRC environment, users can supply a list of nets that need the highest level of accuracy for capacitance extraction. StarRC not only extracts the nets as in the regular flow, but also creates a subset of the design based on the user-specified nets to be extracted using the field solver technology. A merged netlist is generated including the higher-accuracy field solver extracted nets (see Figure 5).
CustomSim Circuit Simulator Integration

Post-layout simulation runtimes are increasing 2-4x with every new process generation. More accurate and efficient parasitic extraction is needed to accelerate simulation and meet tapeout schedules. StarRC offers seamless integration with Synopsys’ industry-leading CustomSim circuit simulator and a wide range of innovative features to boost simulation performance and capacity while preserving signoff accuracy. StarRC’s exclusive interface with CustomSim includes active node extraction, post-layout acceleration with hierarchical back-annotation, and power network optimization. The integration between the two tools enables over 10x simulation performance speed-up for custom IC and memory designs.

Custom AMS Design Platform Integration

StarRC is integrated with Synopsys’ next-generation Galaxy Custom Designer mixed-signal implementation system and with Cadence’s Virtuoso Analog Design Environment (ADE) for custom AMS and custom digital designs. StarRC and Galaxy Custom Designer offer users the unique benefits of an OpenAccess interface combined with the ease-of-use of the familiar Synopsys implementation environment using a common data flow. For the Virtuoso environment, StarRC generates OpenAccess or Cadence DFII database parasitic views for netlisting and simulation, compatible with common netlisting interfaces used within ADE. StarRC offers full probing capabilities for either environment to probe parasitics within the parasitic view or within the matching schematic view (see Figure 6). The parasitic prober allows users to interactively observe point-to-point resistance, total net capacitance, net-to-net coupling capacitance and cross-probing between schematic and parasitic views. It also provides the ability to output probed parasitics to an ASCII report file, and to annotate parasitic view total capacitance values to an associated schematic view.

Figure 5: StarRC integrated fast field solver extraction offers high-accuracy extraction for critical IP within a single extraction environment
Hierarchical Extraction
StarRC’s hierarchical extraction and netlisting offers large transistor-level memory and custom SoC designers a flexible option to improve their post-layout verification productivity. For signoff analysis, flat parasitic extraction with hierarchical back-annotation provides the best combination of accuracy and performance. However, in cases such as reliability analysis, designers may need to extract billions of signal and power net parasitics. Flat parasitic extraction, though most accurate, could be time-consuming in such cases; therefore, designers may prefer hierarchical extraction to speed the parasitic extraction process. Hierarchical extraction may also be preferred in scenarios where design methodologies favor top-down or bottom-up hierarchical design and simulation. StarRC’s hierarchical extraction complements its flat extraction technology by providing optimized hierarchical parasitic data for high-capacity signal and power net analysis.

Variation-aware Extraction
With shrinking technology, parametric yield due to variations in critical device and interconnect process parameters has become the dominant factor in yield loss. In order to improve silicon predictability, it is mandatory that extraction tools model the process variation accurately. Also, as the uncertainty grows, traditional corner-based methodologies requiring multiple process technology files and time-consuming multiple extraction and simulation runs become impractical. Statistical techniques are needed to model these process variation effects.

StarRC offers an advanced statistical solution that enables sensitivity-based parasitic extraction for interconnect process and temperature variation-aware designs. The variation of each process parameter, such as conductor or dielectric thickness, is available through the variation-aware process technology file and is used to compute sensitivities of parasitic values based on each of the process variations.

Figure 6: StarRC integration with custom design environments, such as Galaxy Custom Designer, enables productive cross-probing and simulation debugging.
Process Modeling
- FinFET 3D modeling
- Color-aware double patterning (DPT)
- Trench contact modeling
- 3D-IC, Silicon Interposer TSV modeling
- Litho-aware extraction
- Via etch modeling
- Advanced OPC effect modeling
- CMP simulator interface
- Width- and spacing-dependent thickness variation
- Density-based thickness variation
- Multiple density-based variation
- Width- and spacing-dependent RPSQ variation
- RPSQ variation as function of silicon width
- Nonlinear RPSQ variation
- Trapezoidal polygon support
- Copper interconnect, local interconnect modeling
- Low-K dielectric, silicon on insulator (SOI) modeling
- Conformal dielectric process support
- Support of Air Gap
- Via cap extraction
- Layer ETCH
- Temperature-dependent resistance modeling for conducting layers and vias
- Support of background dielectric
- Nonlinear via resistance modeling
- 45-degree routing support
- Support of multiple inter-layer and intra-layer dielectric
- Support for co-vertical conductors
- Support for non-planarized metal

Productivity and Ease-of-use
- Multi-core processing
- Simultaneous Multi-Corner extraction
- Metal Fill Re-use for ECO TAT reduction
- Incremental extraction
- Hierarchical LVS and ADP extraction flow
- Active node extraction
- Selective device parasitic handling
- Flexible parasitic reduction
- Automated power net extraction optimization (TARGET_PWRA)
- Transparent simulation setup
- License queuing
- User-control reduction of parasitic netlists
- Multiple reduction modes for different applications

Specifications

File Format Support
StarRC supports the following industry-standard formats and interfaces:
- Layout data in: GDSII, LEF/DEF, Milkyway, IC Compiler, IC Validator, Hercules, Calibre
- Output formats: DSPF, SPICE, SPEF, SBPF, SSPEFBinary interface: Direct binary interface to PrimeTime SI (SBPF)

System Requirements
- DRAM: 1GB, recommend 2GB
- Swap Space: 1GB, recommend 4GB
- Installation disk space: 250MB baseline plus 250MB per platform
- Design disk space depends on the circuit size, recommended minimum 500MB

Platform/OS
- IBM RS/6000 AIX (64)
- SPARC Solaris (32)
- SPARC Solaris (64)
- x86 Solaris (32)
- x86 Solaris (64)
- x86 Red Hat Enterprise (32)
- x86 Red Hat Enterprise (64)
- x86 SUSE Enterprise (32)
- x86 SUSE Enterprise (64)

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