

StarRC

Parasitic extraction

Overview

StarRC™ is the EDA industry's gold standard for parasitic extraction. A key component of Synopsys Galaxy™ Implementation Platform, it provides a silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed-signal (AMS) and memory IC designs. StarRC offers modeling of advanced physical effects needed for leading-edge process technologies, including 28-nm. Its seamless integration with industry standard digital and custom implementation systems, timing, signal integrity, power, physical verification and circuit simulation flows delivers unmatched ease-of-use and productivity to speed design closure and signoff verification.

StarRC Solution

Semiconductor process technology has been continually scaling down for the past four decades and the trend continues. Shrinking process geometries, combined with the use of new device structures and an increasing number of metal layers at each new process node, are introducing millions of new parasitic effects in designs. In addition, soaring design sizes and complexities are increasing the sensitivity of circuits to parasitics due to the increasing impact on signal timing, noise and power. To ensure a successful silicon design and meet the tape-out schedules, IC designers need an advanced parasitic extraction solution that delivers signoff accuracy and increased designer productivity. Furthermore, they need a solution that is versatile enough to manage the full design spectrum from custom digital/AMS to full-chip memory and SoC designs.

Synopsys' StarRC is the next-generation high-accuracy and high-performance parasitic extraction solution for digital and custom IC implementation and signoff verification (see Figure 1). Trusted by hundreds of semiconductor companies and proven in thousands of production designs, StarRC provides sub-femtoFarad-accurate technology for design at advanced process technologies. It achieves its high accuracy by performing detailed modeling of device and interconnect parasitic effects in nanometer process technologies. The advanced modeling and accuracy is complemented with the embedded Rapid3D technology for circuits that require even higher field solver accuracy.

StarRC delivers industry-leading performance and capacity for customers' gate-level and transistor-level extraction needs. StarRC's multicore distributed processing technology delivers excellent scalability for efficient utilization of available hardware. Its seamless integration with Synopsys' leading IC Compiler physical implementation solution, gold standard PrimeTime® signoff suite, Galaxy Custom Designer™ mixed-signal implementation solution, IC Validator physical verification solution, CustomSim™ circuit simulation and other third-party implementation and signoff tools enables users to significantly accelerate their design implementation and verification.

The StarRC extraction solution is available in three different configurations: StarRC Custom, StarRC, and StarRC Ultra (see Figure 2). StarRC Custom offers extraction for high-accuracy custom AMS/digital design, StarRC offers full-chip gate-level and transistor-level extraction, and StarRC Ultra offers high-end extraction for advanced analysis flows.

Benefits

- ▶ Flexible multicore technology delivers best-in-class performance and scalability to speed up extraction
- ▶ Advanced process modeling, broadest foundry qualification and proven sub-femtoFarad accuracy increase design predictability. StarRC is trusted by leading foundries to solve modeling challenges at advanced 65-nm to 28-nm process nodes
- ▶ Embedded 20x faster Rapid3D fast field solver technology, built on the gold standard Raphael NXT engine, ensures high-accuracy extraction for critical IP and custom circuits within the single StarRC environment
- ▶ Integration with CustomSim circuit simulation and leading signoff physical verification tools accelerates simulation verification

- ▶ Integration with Synopsys Galaxy Custom Designer and Cadence® Virtuoso® custom design solutions boosts productivity of custom design
- ▶ Binary interchange with PrimeTime timing signoff, as well as seamless integration with Synopsys’ IC Compiler and third-party implementation systems, increases efficiency and reduces design cycle time.

Multicore Processing

Multicore processor hardware has become common due to the widespread need for higher productivity. A large majority of design jobs are run on compute farms consisting of multicore

machines, and IC designers seek design tools that harness the full potential of their hardware network. StarRC’s flexible multicore technology works seamlessly with popular commercial grid computing management software to maximize efficiency across multicore processors, as well as multi-processor compute farms, to take full advantage of available hardware. StarRC offers high performance per CPU core; for example, up to 6x scalability on 8 cores. In addition, StarRC multicore processing consists of easy-to-setup compute resource allocation, automated design partitioning to multiple cores, balanced

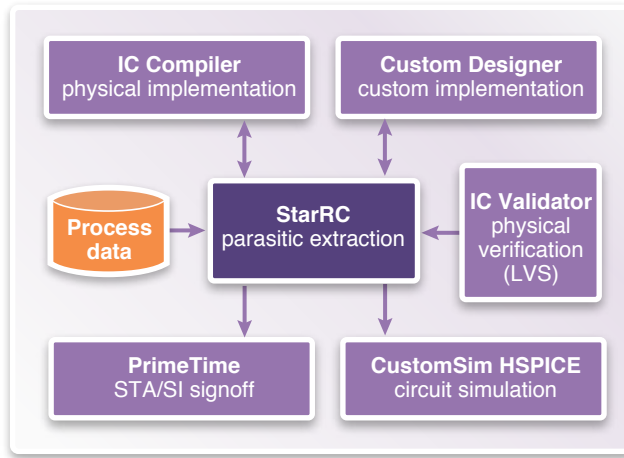


Figure 1: StarRC provides a next-generation parasitic extraction solution for gate-level and transistor-level digital and custom IC designs

Parasitic Extraction Features	StarRC Custom	StarRC	StarRC Ultra
Multicore processing	✓	✓	✓
Advanced process modeling, including 28-nm	✓	✓	✓
Context-specific device parasitic extraction	✓	✓	✓
Integrated fast field solver (high accuracy extraction)	✓	✓	✓
Multi-corner temperature sensitivity extraction	✓	✓	✓
CustomSim circuit simulation integration	✓	✓	✓
Custom layout environment integration	✓	✓	✓
Hierarchical extraction for large transistor-level designs		✓	✓
Full-chip transistor-level and gate-level extraction		✓	✓
Physical implementation interface (Milkyway, LEF/DEF)		✓	✓
PrimeTime binary interface for productivity		✓	✓
Feature-scale (model-based) CMP extraction interface			✓
Variation-aware extraction (statistical random process variation)			✓

Figure 2: StarRC offers flexible product configurations for specific design applications

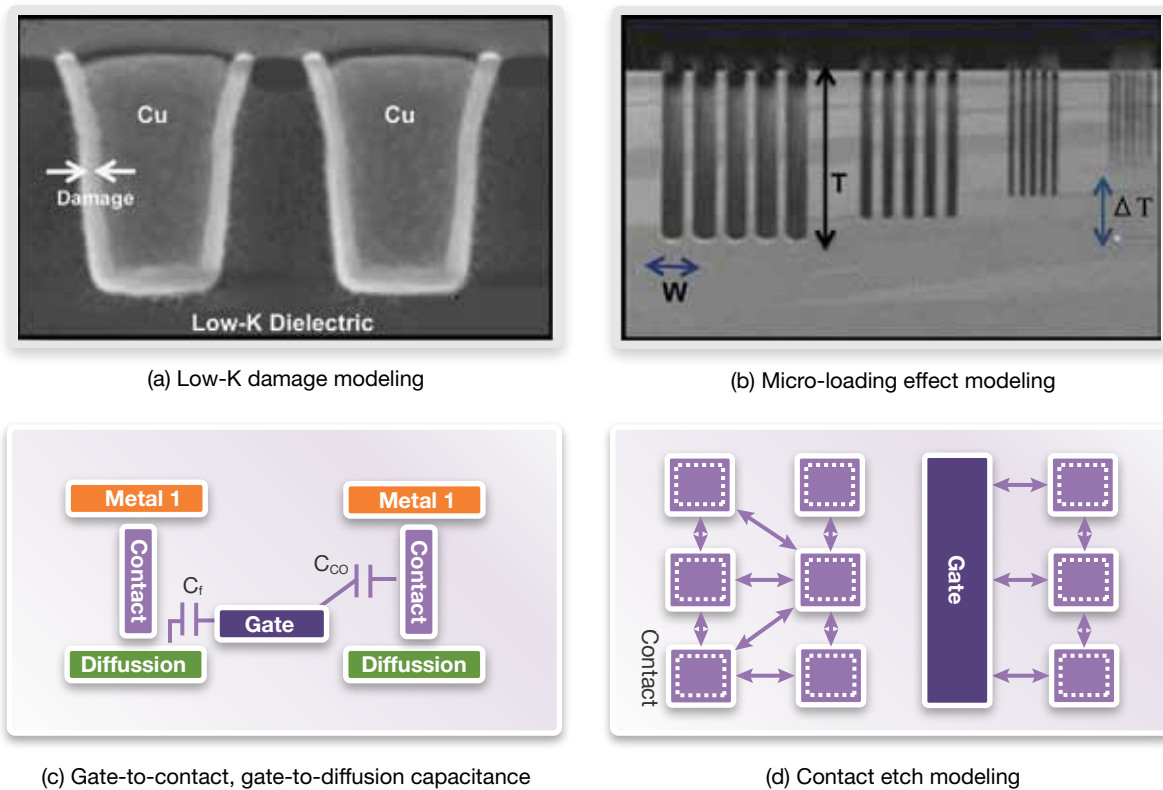


Figure 3: StarRC's advanced interconnect and device parasitic modeling delivers signoff accuracy

load sharing, and automatic failure recovery for a superior fault-tolerant server environment.

Advanced Process Modeling

Increasing process variation and new parasitic effects introduced at each new generation of process technology are significantly increasing design challenges. Advanced process technologies are elevating a variety of physical effects once considered secondary to primary factors affecting circuit behavior, thus increasing the need for accurate modeling to mitigate the chances of silicon failure and lower yields. StarRC delivers a high-accuracy solution for advanced nodes by modeling complex physical effects in smaller geometries and by accounting for every capacitive interaction in design. It extracts millions of capacitors for a typical design; then, using a proprietary parasitic reduction capability, it generates the smallest possible netlist while delivering sub-femtoFarad accuracy.

The nanometer process capabilities offered by StarRC include variation-aware parasitic extraction, litho-aware extraction and chemical-mechanical polishing (CMP)-based thickness variation extraction. The micro-loading effect (bottom thickness variation as a function of conductor width) and low K dielectric damage modeling are two key concerns at sub-45-nm designs due to their profound impact on capacitance. StarRC accurately models these effects for increased extraction and timing accuracy (see Figure 3a, 3b).

At smaller process geometries, device parasitics have an increased impact on circuit behavior, especially in the case of transistor-level circuits. For example, gate-to-contact capacitance can have a significant impact on device performance due to the Miller effect. Device parasitics are becoming "context-specific" at advanced nodes, that is, they are becoming more sensitive to the layout environment

requiring higher levels of accuracy in extraction. StarRC accurately models and extracts the device-level effects such as contact etch effect, gate-to-contact and gate-to-diffusion fringe capacitances for increased signoff accuracy (see Figure 3c, 3d).

High Accuracy Fast Field Solver Extraction

For timing-sensitive circuits such as clock networks, memories, AMS/RF, high-speed digital, standard cells and other IP designs, accuracy is a non-negotiable design criterion. Designers of such critical IP and circuits generally require field-solver-level accuracy as well as fast turnaround time. StarRC offers integrated 3D fast field solver extraction, using Rapid3D technology, for efficient higher-accuracy extraction. Building on the Raphael NXT engine, the brand new Rapid3D technology incorporates the latest advancements in field solver algorithms to deliver 20x faster 3D

extraction while providing the same gold standard accuracy. The embedded Rapid3D technology complements StarRC's primary extraction engine (ScanBand™ technology, explained later under Performance and Capacity) for 3-dimensional self- and coupling-capacitance extraction of critical circuits. Within the single StarRC environment, users can supply a list of nets that need the highest level of accuracy for capacitance extraction. StarRC not only extracts the nets as in the regular flow, but also creates a subset of the design based on the user-specified nets to be extracted using the field solver technology. A merged netlist is generated including the higher-accuracy field solver extracted nets (see Figure 4).

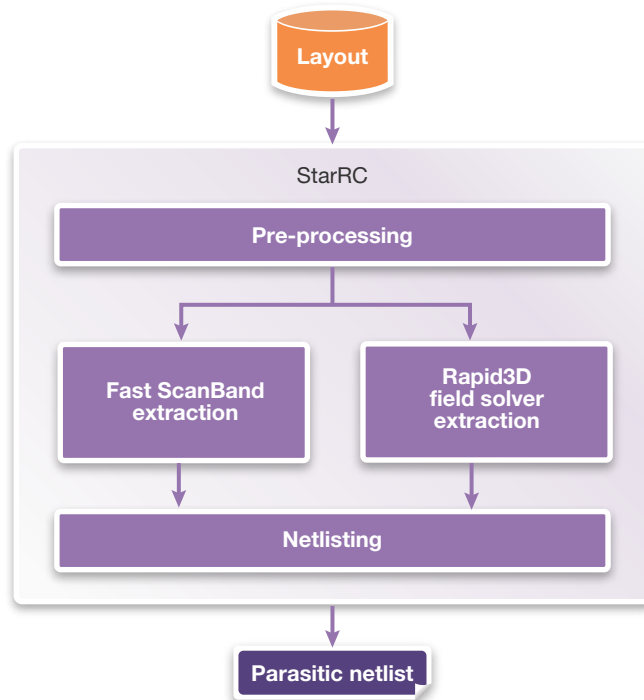


Figure 4: StarRC integrated fast field solver extraction offers high-accuracy extraction for critical IP within a single extraction environment

Multi-corner/Temperature-sensitivity Extraction

As process variation increases and designs become more complex, multiple corner analyses are rapidly increasing in order to ensure maximum certainty of signoff. For instance, designers need multiple interconnect corners for their setup, hold or signal integrity analysis to meet their design specifications. StarRC enhances designer productivity by providing the capability to extract multiple corners in a single run and generating multiple netlists for downstream verification tools.

Besides process variation, temperature variation across a die can have a significant impact on the resistance of a wire and hence the performance and/or functionality of a circuit. StarRC provides an efficient temperature-sensitivity extraction where more than one temperature corner signoff is required. It considers temperature as a variation and writes temperature derating parameters into the extracted netlist for use by the downstream tools. For temperature variation extraction

at the same process corner, StarRC uses standard process technology data and offers near 100% runtime gain by eliminating the need for separate extraction at each additional temperature.

CustomSim Circuit Simulator Integration

Post-layout simulation runtimes are increasing 2-4x with every new process generation. More accurate and efficient parasitic extraction is needed to accelerate simulation and meet tapeout schedules. StarRC offers seamless integration with Synopsys' industry-leading CustomSim circuit simulator and a wide range of innovative features to boost simulation performance and capacity while preserving signoff accuracy. StarRC's exclusive interface with CustomSim includes active node extraction, post-layout acceleration with hierarchical back-annotation, and power network optimization. The integration between the two tools enables over 10x

simulation performance speed-up for custom IC and memory designs.

Custom AMS Design Platform Integration

StarRC is integrated with Synopsys' next-generation Galaxy Custom Designer mixed-signal implementation system and with Cadence's Virtuoso Analog Design Environment (ADE) for custom AMS and custom digital designs. StarRC and Galaxy Custom Designer offer users the unique benefits of an OpenAccess interface combined with the ease-of-use of the familiar Synopsys implementation environment using a common data flow. For the Virtuoso environment, StarRC generates OpenAccess or Cadence DFII database parasitic views for netlisting and simulation, compatible with common netlisting interfaces used within ADE. StarRC offers full probing capabilities for either environment to probe parasitics within the parasitic view or within the matching schematic view (see Figure

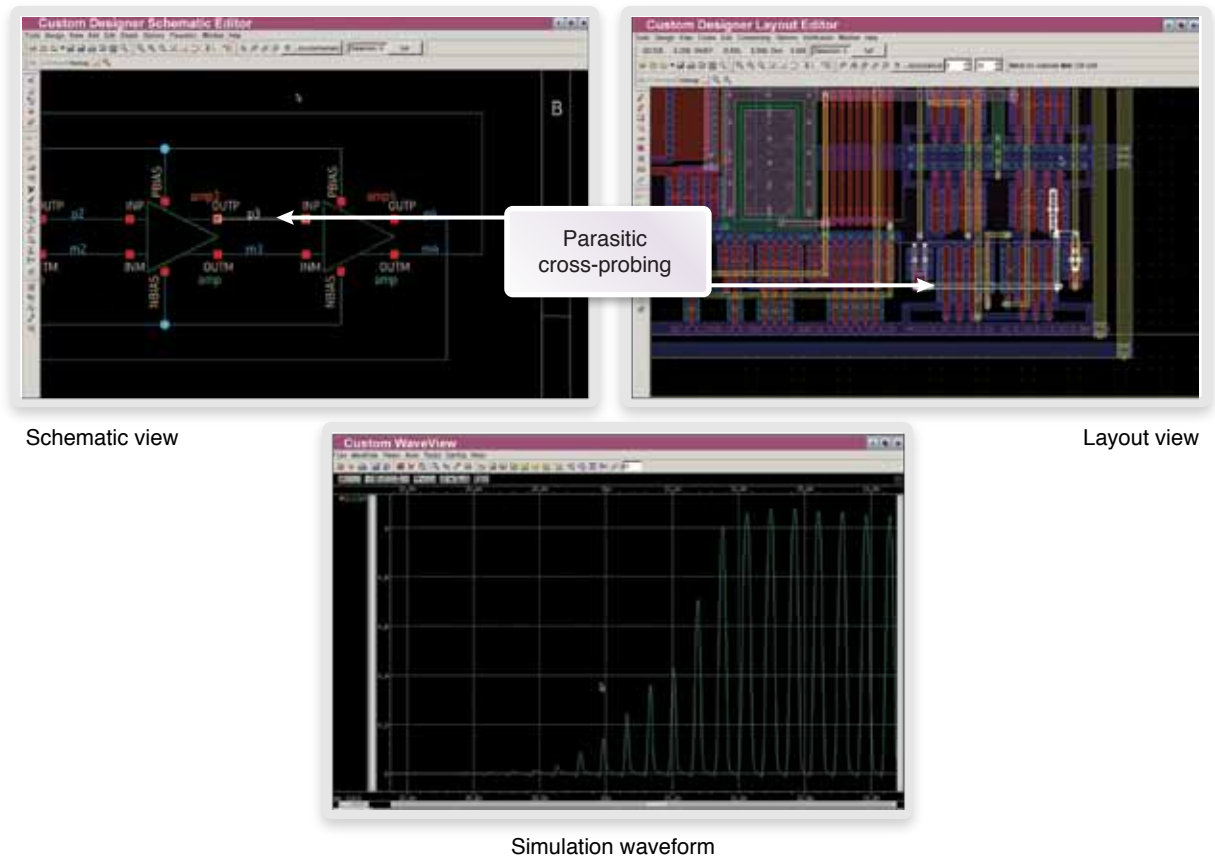


Figure 5: StarRC integration with custom design environments, such as Galaxy Custom Designer, enables productive cross-probing and simulation debugging

5). The parasitic prober allows users to interactively observe point-to-point resistance, total net capacitance, net-to-net coupling capacitance and cross-probing between schematic and parasitic views. It also provides the ability to output probed parasitics to an ASCII report file, and to annotate parasitic view total capacitance values to an associated schematic view.

Hierarchical Extraction

StarRC's hierarchical extraction and netlisting offers large transistor-level memory and custom SoC designers a flexible option to improve their post-layout verification productivity. For signoff analysis, flat parasitic extraction with hierarchical back-annotation provides the best combination of accuracy and performance. However, in cases such as reliability analysis, designers may need to extract billions

of signal and power net parasitics. Flat parasitic extraction, though most accurate, could be time-consuming in such cases; therefore, designers may prefer hierarchical extraction to speed the parasitic extraction process. Hierarchical extraction may also be preferred in scenarios where design methodologies favor top-down or bottom-up hierarchical design and simulation. StarRC's hierarchical extraction complements its flat extraction technology by providing optimized hierarchical parasitic data for high-capacity signal and power net analysis.

PrimeTime Binary Interface

Parasitic netlist size and timing signoff analysis runtime are key concerns for designers of large SoC designs at leading-edge process nodes. The extracted parasitic netlist size of a multi-

million-net design can be as large as several gigabytes of memory that can significantly impact the parasitic read and analysis runtimes. StarRC provides a unique and compact binary parasitic format, called SBPF (Synopsys Binary Parasitic Format), with the industry-leading Synopsys PrimeTime timing signoff tool. SBPF binary interchange format captures identical electrical and connectivity data as SPEF, but offers significant benefits in parasitic netlist size (up to 15x) and reduced parasitic read runtime (up to 80%) while preserving PrimeTime signoff accuracy.

High Full-chip Performance and Capacity

StarRC achieves excellent speed through superior extraction technology. Traditional extraction tools analyze each polygon several times to extract all capacitive coupling. The large quantity

of data is kept in memory by these extraction tools that slow performance considerably without providing an accuracy benefit. StarRC, with its proprietary ScanBand processing technology, analyzes the polygons only once, storing in memory only those polygons which are needed for accurate parasitic extraction. The ScanBand technology enables StarRC to extract large multi-million-instance designs (up to 10 million instances) overnight on a standard 8-16 GB machine.

Variation-aware Extraction

With shrinking technology, parametric yield due to variations in critical device and interconnect process parameters has become the dominant factor in yield loss. In order to improve silicon predictability, it is mandatory that extraction tools model the process variation accurately. Also, as the uncertainty grows, traditional corner-based methodologies requiring multiple process technology files and time-consuming multiple extraction and simulation runs become impractical. Statistical techniques are needed to model these process variation effects.

StarRC offers an advanced statistical solution that enables sensitivity-based parasitic extraction for interconnect process and temperature variation-aware designs. The variation of each process parameter, such as conductor or dielectric thickness, is available through the variation-aware process technology file and is used to compute sensitivities of parasitic values based on each of the process variations.

Reluctance (Inductance) Extraction

Inductance effects become more prominent as the resistance (both device and interconnect) decreases and the operating frequency increases. At low frequencies, RC modeling is sufficient and inductance can safely be ignored. As clock frequencies increase, however, modeling of global interconnects such as RC circuits is no longer adequate and inductance must be included in the modeling. Ignoring the inductance effect can underestimate signal integrity problems as well.

StarRC provides a novel approach to modeling on-chip inductance effects, called partial reluctance extraction. Reluctance is defined as the inverse of inductance. Reluctance effects are localized just like capacitance and unlike inductance, resulting in a much sparser matrix compared to inductance. This enables StarRC to produce the smallest netlist without losing any accuracy, overall achieving orders of magnitude faster extraction and simulation.

Other Key Features

Process Modeling

- ▶ Litho-aware extraction
- ▶ Via etch modeling
- ▶ Advanced OPC effect modeling
- ▶ CMP simulator interface
- ▶ Width- and spacing-dependent thickness variation
- ▶ Density-based thickness variation
- ▶ Multiple density-based variation
- ▶ Width- and spacing-dependent RPSQ variation
- ▶ RPSQ variation as function of silicon width
- ▶ Nonlinear RPSQ variation
- ▶ Trapezoidal polygon support
- ▶ Copper interconnect, local interconnect modeling
- ▶ Low-K dielectric, silicon on insulator (SOI) modeling

- ▶ Conformal dielectric process support
- ▶ Support of Air Gap
- ▶ Via cap extraction
- ▶ Layer ETCH
- ▶ Temperature-dependent resistance modeling for conducting layers and vias
- ▶ Support of background dielectric
- ▶ Nonlinear via resistance modeling
- ▶ 45-degree routing support
- ▶ Support of multiple inter-layer and intra-layer dielectric
- ▶ Support for co-vertical conductors
- ▶ Support for non-planarized metal

Productivity and Ease-of-use

- ▶ Incremental extraction
- ▶ Hierarchical LVS and ADP extraction flow
- ▶ Active node extraction
- ▶ Selective device parasitic handling
- ▶ Flexible parasitic reduction
- ▶ Automated power net extraction optimization (TARGET_PWRA)
- ▶ Transparent simulation setup
- ▶ License queuing
- ▶ User-control reduction of parasitic netlists
- ▶ Multiple reduction modes for different applications

Specifications

File Format Support

StarRC supports the following industry-standard formats and interfaces:

- ▶ Layout data in: GDSII, LEF/DEF, Milkyway, IC Compiler, IC Validator, Hercules, Calibre
- ▶ Output formats: DSPF, SPICE, SPEF, SBPF, SSPEF
- ▶ Binary interface: Direct binary interface to PrimeTime SI (SBPF)

System Requirements

- ▶ DRAM: 512MB, recommend 1GB
- ▶ Swap Space:512MB, recommend 2GB
- ▶ Installation disk space:250MB baseline plus 250MB per platform
- ▶ Design disk space depends on the circuit size, recommended minimum 500MB

Platform/OS

- ▶ IBM RS/6000 AIX (64)
- ▶ SPARC Solaris (32)
- ▶ SPARC Solaris (64)
- ▶ x86 Solaris (32)
- ▶ x86 Solaris (64)
- ▶ x86 Red Hat Enterprise (32)
- ▶ x86 Red Hat Enterprise (64)
- ▶ x86 SUSE Enterprise (32)
- ▶ x86 SUSE Enterprise (64)

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