Synopsys and STMicroelectronics
TetraMAX Small Delay Defect ATPG Boosts Test Quality at STMicroelectronics

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Philippe Magarshack
Group Vice President and Central CAD & Design Solutions General Manager, STMicroelectronics

Business
STMicroelectronics is a global leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications.

Challenges
‐ Achieving very high test quality goals across product lines
‐ Maintaining low cost of manufacturing tests and diagnostics
‐ Implementing test quality improvements without impacting tapeout schedules

Solution
‐ TetraMAX ATPG® for small delay defect testing
‐ DFT MAX compression
‐ PrimeTime® static timing analysis

Benefits
‐ Higher test quality resulting in much fewer test escapes than previously possible
‐ Lower test escape costs
‐ No impact on design schedules

Overview
STMicroelectronics was faced with the challenge of meeting very high corporate test quality objectives across all its product lines without increasing test costs. This challenge was made even more difficult since on-chip process variations are more pronounced in today’s manufacturing processes, resulting in more small delay defects (SDDs). SDDs are subtle manufacturing defects that add enough signal-propagation delay in a device to produce failures at the targeted frequency.

Test engineers at STMicroelectronics were aware that targeting SDDs during manufacturing test might be an effective way to improve defect coverage and lower defective parts per million (DPPM). However, accurate timing information is needed to create tests that reliably detect the small added delays, so SDD testing was considered infeasible due to its computational overhead.

But breakthrough timing-aware technology in TetraMAX automatic test pattern generation (ATPG) enabled designers at the company to use precise timing information generated by Synopsys’ PrimeTime static timing analysis, the industry’s de-facto signoff solution, to quickly and easily generate patterns that target SDDs.
A key advantage of Synopsys’ approach to SDD ATPG is that it leverages PrimeTime static timing analysis, which is widely used at STMicroelectronics. TetraMAX’s ability to import pin slacks generated by PrimeTime to target small delay defects with very high precision is critical to improving test quality over standard transition delay ATPG.”

Roberto Mattiuzzo
Digital Test Solutions Manager, Central CAD and Design Solutions, Front-End Technology Manufacturing, STMicroelectronics

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Silicon Testing Results
To assess the viability of Synopsys’ SDD ATPG technology, test engineers at STMicroelectronics collected test from hundreds of thousands of parts using four fundamental types of tests: stuck-at, static bridging, dynamic bridging and delay tests. The delay tests were composed of standard transition delay patterns and SDD patterns. The data indicated that about 94.5% of all failing parts were covered by the delay tests, and that 20% of failing parts were covered only by the delay tests.

Upon examining the data for the 20% of defective parts covered only by the delay tests, they observed that 63% of these parts were covered only by the SDD patterns. The remaining 37% covered by transition delay patterns were also covered by SDD patterns.

STMicroelectronics observed similar results after more testing: “Extensive silicon testing results at STMicroelectronics has proven that Synopsys’ TetraMAX ATPG patterns targeting small delay defects consistently screen more failures than the other types of test we use today in production,” said Philippe Magarshack, group vice president and Central CAD & Design Solutions general manager, at STMicroelectronics.

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A Winning Strategy
Because Synopsys’ SDD ATPG solution is easy to implement and built into STMicroelectronics’ existing Synopsys implementation flow, the new capability has been widely adopted across design groups at STMicroelectronics, improving the quality of production testing and lowering the costs of test. “The step increase in test quality due to small delay defect testing has significantly boosted our DPPM reduction program since deployment of Synopsys’ small delay defect ATPG capability to design teams,” said Philippe Magarshack.