

# DFTMAX Compression

## High Quality, Low Cost Test

### Overview

*DFTMAX™ compression is a comprehensive test compression solution that addresses the cost challenges of testing complex designs, particularly when fabricated with small process technologies. These deep-submicron (DSM) designs can have subtle manufacturing defects that are only detected by applying DSM tests, such as at-speed and bridging tests, in addition to stuck-at tests. The extra patterns needed to achieve high test quality for these designs can increase both the test time and the test data, resulting in higher test costs.*

*DFTMAX compression reduces these costs by delivering push-button 10-100x test data and test time compression with very low silicon area overhead. Seamlessly enabling compression in TetraMAX® ATPG, and encapsulated in Synopsys' Galaxy™ Design Platform, DFTMAX compression achieves predictable results with virtually zero impact on timing.*

### Key Benefits

- ▶ Lowers test costs
- ▶ Provides high defect coverage
- ▶ As easy-to-use as standard scan
- ▶ Avoids any impact on design timing
- ▶ Leverages physical design for area optimization
- ▶ Minimizes area impact
- ▶ Minimizes required number of test pins
- ▶ Preserves low-power design intent
- ▶ Minimizes power consumption during test

### Key Features

- ▶ 10-100x test time and test data reduction (typical)
- ▶ Based on patented, powerful adaptive scan technology
- ▶ Built-in to synthesis and ATPG – easy to implement as standard scan
- ▶ Multicore compute platform support
- ▶ Integrated with Design Compiler® Topographical Technology and IC Compiler for concurrent optimization of area, power, timing, physical and test constraints
- ▶ Comprehensive test DRC analysis
- ▶ Hierarchical scan synthesis flow support
- ▶ Pin-limited test optimizations
- ▶ Unknown logic value (X) handling
- ▶ Flexible scan channel configurations to support multi-site testing and wafer-level burn-in
- ▶ Multiple compression configurations to support different testers and packages with different I/O
- ▶ Boundary scan synthesis, 1149.1/6 compliance checking and BSDL generation
- ▶ Enables TetraMAX ATPG for quick compressed pattern generation

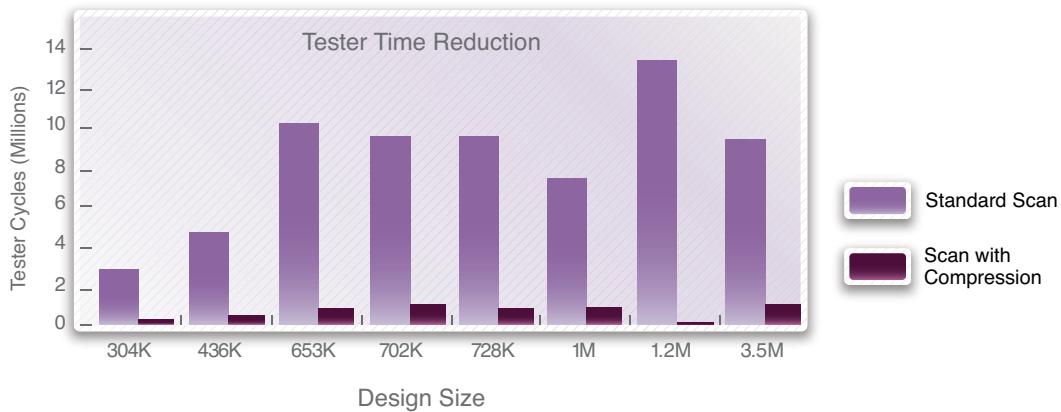


Figure 1: DFTMAX compression delivers 10-100X test time and test volume reduction

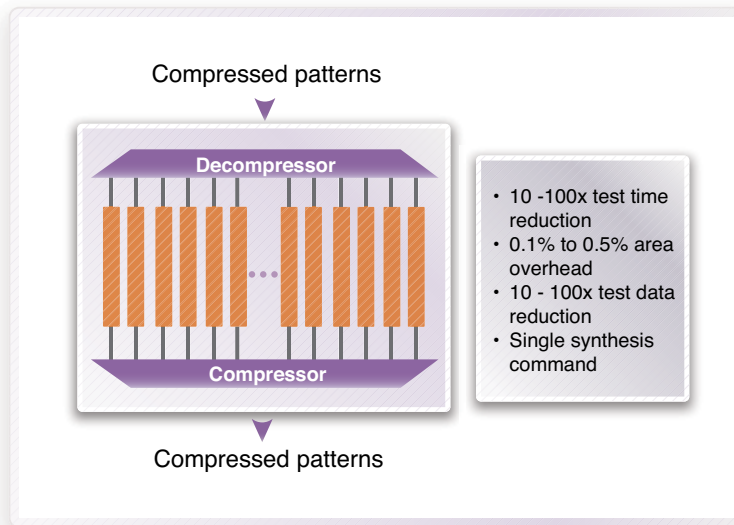


Figure 2a: DFTMAX Compression

### DFTMAX Compression Delivers 10-100x Test Time and Test Volume Reduction

DFTMAX compression reduces the costs of nanometer testing by providing 10-100x test data volume compression (Figure 1). Using Synopsys' patented "adaptive scan" compression architecture, DFTMAX compression saves test time and makes it possible to include DSM test patterns in tester configurations where memory is limited. With the industry's most area-efficient solution, DFTMAX compression has virtually no impact on design timing and results in the same high test coverage as provided by standard scan (Figure 2a).

### Pin-Limited Test

To accommodate designs that require a limited number of test data pins either at the top-level or per core, DFTMAX compression generates an optimized architecture that ensures high quality without incurring extra test data. Several current trends that are limiting the number of available test pins include tighter form factors, multi-site testing to target multiple die simultaneously, and core-based methodologies with multiple embedded compressor-decompressors (CODECs). These types of techniques minimize the number of chip-level test pins available to each CODEC. To provide up to one hundred times test

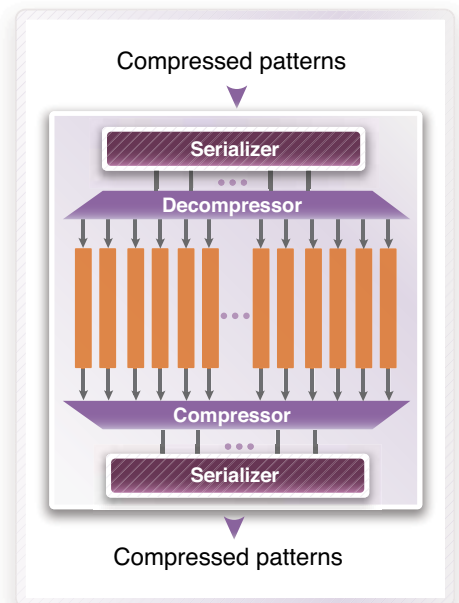


Figure 2b: DFTMAX Compression for pin-limited test

data volume and test application time reduction for these pin-limited test applications, DFTMAX compression generates a high-speed, low-pin tester interface that automatically serializes the test data (Figure 2b).

### Test Compression Synthesis

The DFTMAX compression synthesis flow is practically the same as the industry’s most widely deployed standard scan synthesis flow enabled by DFT Compiler. DFTMAX compression synthesizes test compression directly from RTL to testable gates with full optimization of synthesis design rules and constraints. All test and compression requirements specified prior to the synthesis process are met concurrently with area, timing and power optimization. DFTMAX compression synthesizes the design at the gate-level with all scan design rules checked and the test and compression logic verified, leading to very high and predictable test coverage and test compression results. The implementation of DFT, including test compression, within the design synthesis environment allows problems to be found and fixed earlier in the design cycle, thus avoiding ‘schedule-breaking’ design iterations. DFTMAX compression also enables TetraMAX ATPG to seamlessly generate compressed test patterns having the highest test quality.

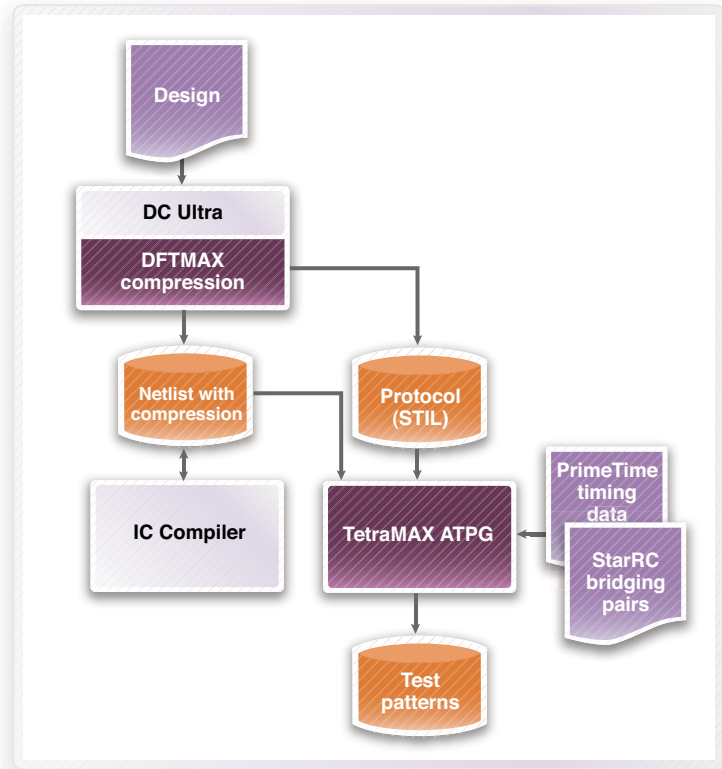


Figure 3: Test compression flow

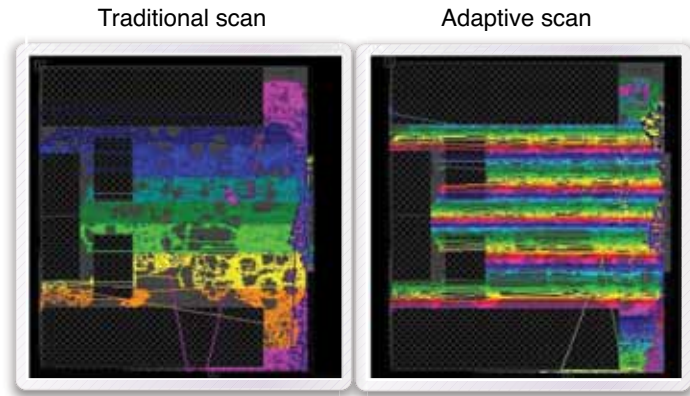


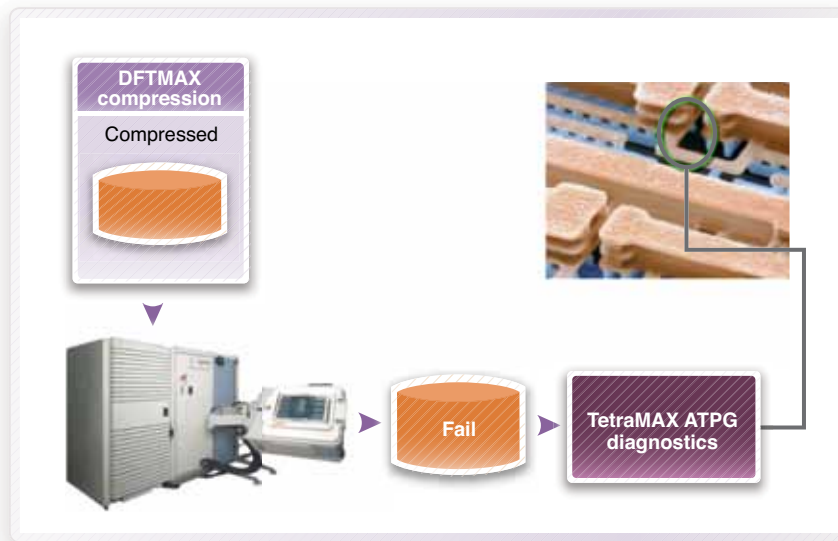
Figure 4: These screen captures show DFTMAX compression results without the routing congestion associated with standard scan

### Integration With Galaxy Design Platform For Concurrent Optimization Of Area, Power, Timing, Physical And Test Constraints

With Synopsys’ unique synthesis flow (Figure 3), adaptive scan compression logic is synthesized simultaneously with scan chains within the Galaxy Design Platform. Topographical scan chain ordering and partitioning provides

excellent timing and area correlation with physical results using IC Compiler. This enables designers to achieve area, power, timing and DFT closure simultaneously. DFTMAX compression writes detailed scan chain information which IC Compiler then reads to perform further optimizations to reduce area impact and decrease overall routing congestion (Figure 4).

Integrating DFT resources into a complex multi-voltage design can be a time-consuming and error-prone process without automation tailored for low-power flows. Once voltage domain characteristics of the design with IEEE 1801 (unified power format) are specified, DFTMAX compression automatically inserts level shifters and isolation cells during scan chain



**Figure 5: DFTMAX compression fully supports proven TetraMAX ATPG ATE links for an effective and accurate yield diagnostics solution**

implementation. To reduce routing congestion and area impact of the DFT logic, DFTMAX compression minimizes both scan chain crossings between power/voltage domains and the number of level shifters inserted.

### Complete DFT Rules Checking

DFTMAX compression enables designers to create “test-friendly” RTL. It identifies DFT rules violations early in the design cycle during the pre-synthesis stage to avoid design iterations. The DFT rules checker validates that the design is compliant with scan rules leading to ensure operational scan chains and the highest test coverage. The violations can be debugged using a graphical browser in Design Vision. It has comprehensive rules checks for:

- ▶ Violations that prevent proper scan operation
- ▶ Violations that prevent data capture
- ▶ Violations that lower fault coverage

The same TetraMAX ATPG DRC engine is run from RTL to gate level, making it possible for designers to validate

testability all the way through the design synthesis process.

### Hierarchical Scan Synthesis

To handle test synthesis of very large designs, some level of abstraction is required so that the system/chip integrator can reduce design time. By abstracting the DFT information in a test model, along with timing and placement information, DFTMAX compression enables quick hierarchical test implementation of multi-million gate designs.

### Boundary Scan Synthesis And Compliance Checking To The 1149.1/6 Standard

DFTMAX compression delivers a complete set of boundary scan capabilities including:

- ▶ TAP and BSR synthesis
- ▶ Compliance checking to the IEEE 1149.1/6 standard
- ▶ Boundary Scan Description Language (BSDL) file generation
- ▶ Functional and DC parametric pattern generation for manufacturing test

### Transparent Integration In TetraMAX ATPG For Power-Aware Test

DFTMAX compression transfers all information about the adaptive scan compression architecture and test operation to TetraMAX ATPG. Working together, TetraMAX ATPG and DFTMAX compression automatically generate compressed, power-aware test patterns with highest test coverage.

### Integration With TetraMAX ATPG Diagnostics

DFTMAX compression fully supports proven TetraMAX ATPG ATE links for failure diagnosis and delivers a straightforward flow from tester fail to location of the defect. DFTMAX compression and TetraMAX ATPG diagnostics together deliver a very effective and accurate yield diagnostics solution (Figure 5). For fast resolution of yield issues, the diagnostics data from TetraMAX ATPG can be automatically read and analyzed by the Yield Explorer yield management system.