

# DFT Compiler

## Standard Scan Synthesis

### Overview

**DFT Compiler - Synopsys' design-for-test (DFT) synthesis solution – delivers scan DFT transparently within Synopsys' synthesis flows with fastest time to results. DFT Compiler's integration with Design Compiler® and IC Compiler ensures DFT with optimization of area, power, and timing constraints, and predictable timing closure of physically optimized scan designs. DFT Compiler enables designers to conduct in-depth testability analysis at the register transfer level (RTL) to implement the most effective test structures at the hierarchical block level, and, if necessary, to automatically repair test design rule checking (DRC) violations at the gate-level. DFT Compiler is compatible with Synopsys' patented DFT MAX compression for flows delivering high quality test compression, resulting in higher designer productivity.**

### Key Features/Benefits

- Correlated standard scan synthesis
- Shortens the design cycle, eliminating design iterations and schedule risks
- Increases productivity, accounting for testability early in the design
- Supports low power and multi-voltage flows
- Integrated with Design Compiler Topographical Technology for highest correlation of area and timing with physical results using IC Compiler
- Creates STIL protocol file automatically for input to TetraMAX® ATPG

### Test DRC

- Ensures fast, accurate testability assurance
- Delivers feedback on testability violations in source-code browser
- Estimates fault coverage
- Links Test DRC analysis with Design Vision graphical user interface

### AutoFix

- Enables automatic repair of Test DRC violations at the gate-level

### Rapid Scan Synthesis Technology

- Enables rapid implementation of the most effective test structures at the hierarchical block level
- Hierarchical scan synthesis using test models facilitates multimillion-gate capacity

### Correlated Standard Scan Synthesis

In DFT Compiler (Figure 1), scan logic is synthesized directly from the RTL to testable gates with full optimization of synthesis design rules and constraints. This means that all the necessary test requirements have been specified prior to the synthesis process. DFT Compiler supports low power, multi-voltage design flows, and creates a gate-level implementation that is fully scannable and meets all design constraints and process technology rules, including test. The final design that comes out of synthesis is "ATPG-ready" with all test logic verified and scan design rules checked, leading to very high and predictable test coverage results. Moreover, integration with Design Compiler Topographical Technology provides the highest possible predictability of area and timing results with IC Compiler. This ensures problems will be found and fixed earlier in the design cycle, thus avoiding 'schedule-breaking' design flow iterations. DFT Compiler also generates the test protocol in STIL format that feeds directly into TetraMAX ATPG.

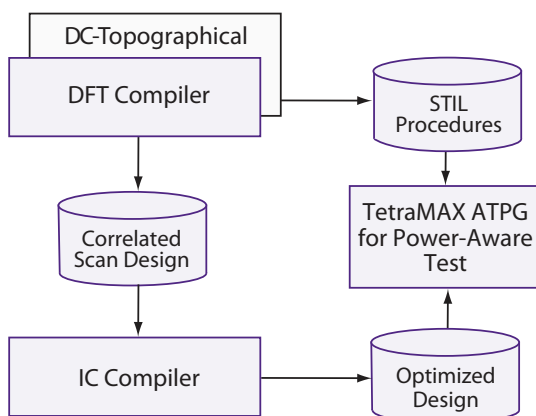


Figure 1: The Integrated DFT Compiler and IC Compiler Flow

Topographical scan chain ordering and partitioning provides excellent timing and area correlation with physical results using IC Compiler. This enables designers to achieve area, power, timing and DFT closure simultaneously. DFT Compiler writes detailed scan chain information to the Synopsys design database which IC Compiler then reads to perform further optimizations to reduce area impact and decrease overall routing congestion.

The tight integration of scan synthesis within IC Compiler enables designers to achieve

- Faster timing closure with testable designs
- Decreased overall routing congestion
- Minimized timing violations related to scan routing

### Test DRC

With traditional design methodologies, test-related problems might not show up until late in the design cycle. Fixing testability violations at the gate-level negatively impacts overall design productivity. Test DRC enables the designer to create “test-friendly” RTL that can then be easily synthesized in the DFT synthesis environment. The primary function of Test DRC is to provide feedback on the testability of the design during the pre-synthesis stage. The module designer invokes the Test DRC feature on the RTL module prior to synthesis to verify a comprehensive set of pre-scan DRC rules. The designer has the option to fix the violations in the RTL source code based on the feedback. This enables the designer to account for RTL testability early in the design process. The feedback on violations can be viewed through a browser in the Design Vision graphical user interface (Figure 2).

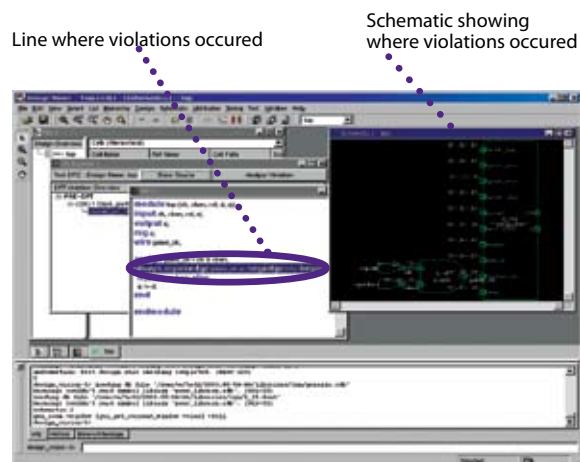


Figure 2: DFT GUI showing Test DRC violations and schematic

A majority of rules checked by Test DRC are pre-scan DRCs that comprehensively cover the following set of violations:

- Violations that prevent scan insertion (e.g., uncontrollable clock or asynchronous set/reset to a flip-flop)
- Violations that prevent data capture (e.g., clock signal drives data pin of flip-flop)
- Violations that reduce fault coverage (e.g., combinational feedback loops)

### AutoFix

While Test DRC enables designers to identify violations at the RT level, the designer has also the option to let the AutoFix capability fix these violations at the gate level during the synthesis stage, while meeting timing constraints. AutoFix focuses primarily on the controllability of clocks and asynchronous set/reset signals, since these are some of the most common testability problems. After DRC violations, the designer uses the AutoFix capability to automatically insert test logic at the gate-level to fix these violations. It ensures that the netlist is testable and ready for ATPG. Since AutoFix is integrated within DFT synthesis, the testability fixes have minimal or no impact on the overall timing and area constraints of the design. Figure 3 shows an example circuit with uncontrollable clock and asynchronous reset inputs to a bank of flip-flops. These are gross DRC violations, which will drastically reduce the test coverage. AutoFix has also been extended to support the testing of shadow logic around embedded memory modules (Figure 4). Using this capability, called shadow-logic DFT, the designer can synthesize testability logic at the memory module I/O to enhance the controllability and observability of the shadow logic around the embedded memory module. The

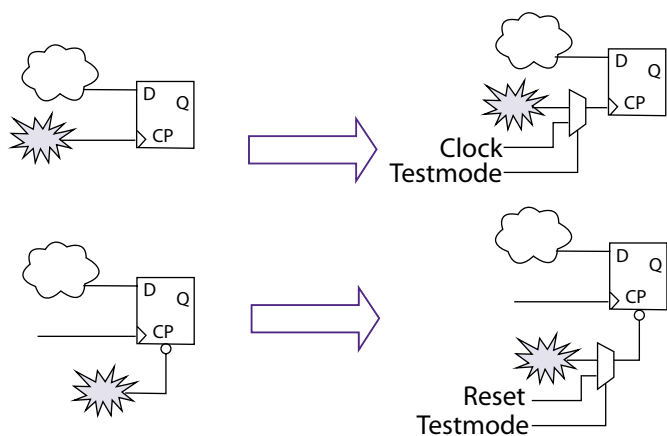


Figure 3: Automatic repair of scan rule violations

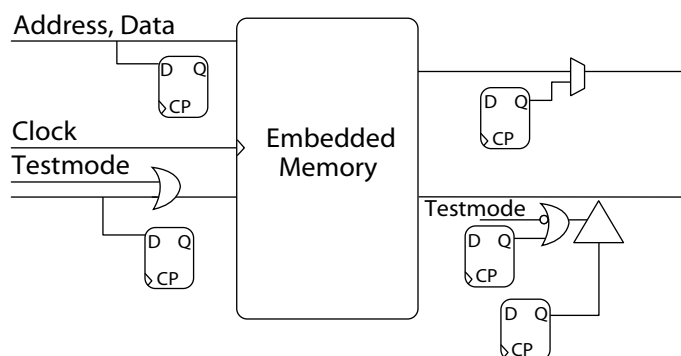


Figure 4: Shadow-Logic DFT for an Embedded Memory

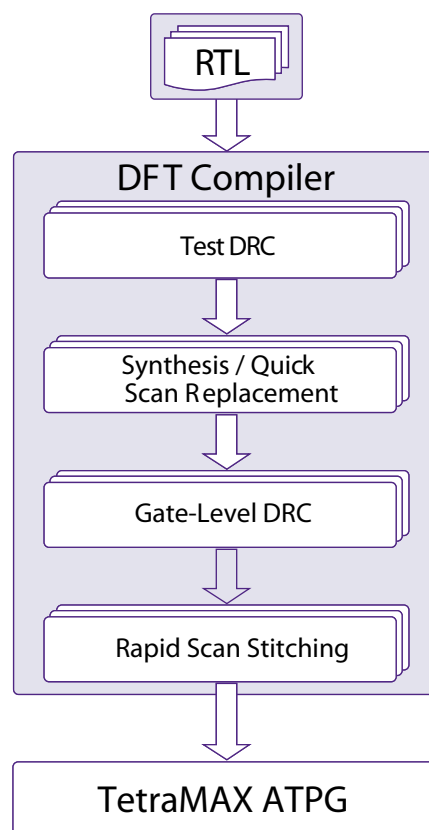


Figure 5: Rapid Scan Synthesis Flow

DFT driven placement capability in IC Compiler places the newly inserted testability logic closer to the respective ports to minimize congestion.

**Rapid Scan Synthesis**

Rapid Scan Synthesis flow (Figure 5) can be used where the full optimization capabilities of DFT Synthesis is not desired to implement a quick prototype of the scan architecture.

This capability enables the rapid implementation of scan chains and DFT logic to create correct-by-construction scan chains both in the logical as well as physical environments to generate a scan netlist to be handed over to ATPG for an early estimate of test coverage or test pattern count.

To handle the test synthesis of large designs at the chip level, some level of abstraction may be desirable so the system/chip

integrator can further reduce design time. By abstracting the DFT information in a test model, along with timing and placement information, the designer can make fundamental DFT decisions very early on.

**Transparent Integration With TetraMAX ATPG for Power-Aware Test**

DFT Compiler transfers all information about the scan chains to TetraMAX ATPG to automatically generate power-aware test patterns with the highest test coverage. DFT Compiler is compatible with all TetraMAX ATPG engines and DSM fault models.

**For information related to products, training or support services, please visit the Web at [www.synopsys.com](http://www.synopsys.com).**

**For sales assistance, call 1 650 584 5000.**



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