

DFTMAX™ Compression Backgrounder

Maximum Test Cost Reduction

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Introduction

DFTMAX compression addresses the dual requirements of high test quality and low test cost. These requirements can be met even as chip designs become larger and new process technologies introduce more complex failure modes.

To decrease test costs while preserving design quality of results and established design flows, DFTMAX compression generates a powerful scan architecture that offers a 100x and more reduction in test application time and test data volume.

Because DFTMAX compression is built into the Synopsys Galaxy Implementation platform, designers implement scan compression predictably without affecting the functional, timing, or power requirements of the design. Combined with the powerful Synopsys TetraMAX® automatic test pattern generator (ATPG), DFTMAX compression provides a complete range of design rule checking (DRC), synthesis, integration, pattern generation, verification, and diagnostics capabilities.

Utilizing Synopsys patented “adaptive scan” technology, DFTMAX compression has successfully lowered test costs across a large variety of semiconductor designs. Since its inception, adaptive scan has overtaken the use of traditional standard scan delivered by Synopsys. In the following we take a closer look at this evolution of the adaptive scan technology delivered in the DFTMAX compression.

Standard Scan

The EDA industry has constantly faced the challenge of delivering ATPG technology that produces high fault coverage with fewer test manufacturing patterns. Each new technology included advances in pattern generation and fault simulation algorithms that have primarily targeted standard scan. The maturing process of scan test technology and methodology took about 40 years with the most significant event being the adoption of standard scan into the synthesis flow. The critical weakness of standard scan was the fact that the growth of the flip-flop count over the generations of design had been continuously outpacing the growth in the scan terminals (i.e. scan input and scan output pins) available for the designs.

Evident over the years is that the number of flip-flops increases with the design size (Figure 1). With a relatively constant number of scan terminals these flip-flops are distributed across the same number of scan chains making the scan chains longer. The test application time of a scan test, comprised of a shift operation followed by a capture cycle, increases along with this effect. The test data volume also increases as every flip-flop accounted for one stimulus value and one observed value. The increased test time and data increase was a negative attribute on the stellar record of standard scan technology.

Simplicity is the most important feature of standard scan technology. Standard scan is easy to understand, implement, and use.

In spite of its shortcomings, there are excellent features of scan technology. The most important feature of scan technology is that it is simple. The simplicity is multi-dimensional – scan is easy to understand; scan is easy to implement; and scan is easy to use. Because of this simplicity, Synopsys has been able to blend scan into design flows without disrupting important layout and timing convergence of the design. Scan also has the following features that are now considered matter of fact:

- ▶ Scan has “low” area overhead. While this may contradict the traditional thinking on the subject, the reality is that scan plays a critical design function – its area requirements are acceptable and not overhead.
- ▶ Scan adds only combinational logic to the existing edge triggered flip-flops in the design to construct scan chains.
- ▶ Scan does not require changes in the netlist for blocking unknown values (Xs) in the design. An unknown response of the circuitry during test does not inhibit the application of the test itself.

Evolution of Standard Scan

With so many positive aspects of standard scan, scan itself should not be abandoned to solve the problem of increased test data volume and test application time caused by the excessively long scan chains. This goal was the driver of “adaptive scan” technology. In contrast, the initial commercial approaches to address the problems involved complex IP in the scan path that relied on sequential logic to supply test stimulus to and retrieve test responses from many short internal chains in the design with a small scan interface. With a conceptual breakthrough in changing the stable control signal of scan chains to be one that changes on a per-shift basis the first generation of adaptive scan was born.

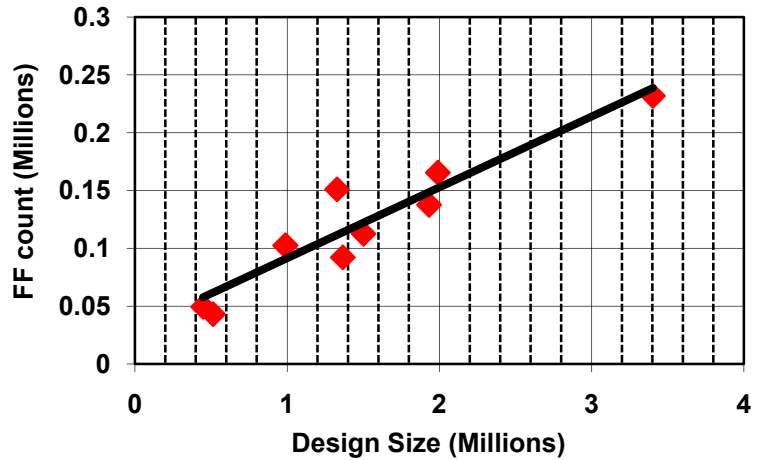


Figure 1 - Increasing flip-flop count vs. design size

Adaptive Scan – Version G1

Powerful Simplicity

Unlike other compression schemes, adaptive scan has multiplexers in the logic that sits between the scan inputs and the internal chains (this logic is usually referred to as the “decompressor”). These multiplexers provide different alliances between the internal chains and the driving scan inputs. Since the relationship between the scan chain and the scan input remain the same as scan design, the compression architecture retains all the characteristics of scan. In Figure 2 - The adaptive scan architecture implemented without the X-masking scheme, there are two scan-in pins, two scan-out pins, and a decompressor with three configurations as represented by

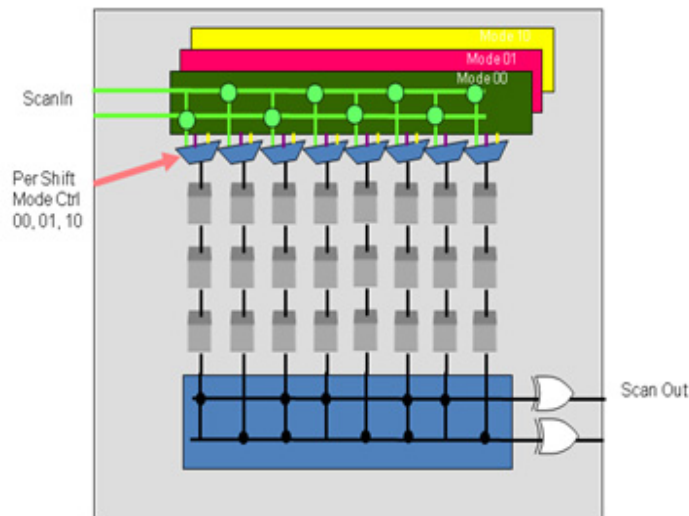


Figure 2 - The adaptive scan architecture implemented without the X-masking scheme

the colors green, red, and yellow. When the multiplexer control signals are set to the binary value “00”, the odd numbered chains are connected to one scan-in pin and the even numbered chains are connected to the other scan-in pin. The other two configurations (control signals set to “01” and “10”) are depicted by color, but not shown in their state. The architecture itself relies on the connections within a configuration and across configurations being as independent of each other.

The logic between the scan chains and the scan outputs is called the “compressor”. Since exclusive-OR (XOR) logic provides the highest observability, it is the most popular choice for any compression scheme for the compressor. In adaptive scan, the XOR logic is designed with redundant connections to tolerate unknown values (Xs) in the test response and provide unique encoding for each scan chain’s values at the scan outputs for diagnostics.

The first generation adaptive scan comes with several options. The most important option is the mask logic between the internal scan chains and the XOR circuitry. The mask logic prevents the capture values of certain scan chains entering the decompressor circuitry. This is particularly valuable for preventing Xs from propagating. The mask select control is combinational logic, making it straightforward to understand.

With the feedback from customer production experience with DFTMAX compression, features were added and several benefits became noteworthy. While adaptive scan provided competitive test application time reduction (TATR) and test data volume reduction (TDVR), the area footprint was measured to be extremely small. Some features reduced layout congestion while others allowed for efficient hierarchical implementations. Being combinational, light weight, and implemented with the widely deployed Design Compiler synthesis tool allowed for a very fast deployment of the technology in existing scan flows.

Adaptive Scan – Version G2

For many designs, adaptive scan version G1 required approximately 8 scan input terminals for optimal ATPG results. The growing trend of multisite testing, core-based methodology, and limited digital pin designs established the need for a minimum number of scan terminals – as few as one input and one output terminal. Testing with few terminals is commonly referred to as pin-limited test. Adaptive scan version G1 supports pin-limited test, but the results are not always predictable. This drove adaptive scan development towards a new version.

To address pin-limited test, adaptive scan version G2 was created. This version leverages concepts of pipelining that have been previously used in standard scan technology. Using pipelining flip-flops allows matching 1) the limited number of available scan terminals and 2) the desired pin width of compressor-decompressor (CODEC). This G2 scheme for pin-limited test allows the original strengths of adaptive scan to be retained.

To illustrate adaptive scan version G2 and its roots in version G1, refer to Figure 3. The illustration shows two cores of the adaptive scan implemented with pipelining (or serialized) flip-flops to allow for a one terminal interface to the compression scheme. While the scan chains no longer look contiguous the patterns and the behavior of the overall compression circuitry for the user, ATPG, and fault simulation algorithm remains similar to that of scan - hence, achieving the overall goal of simplicity.

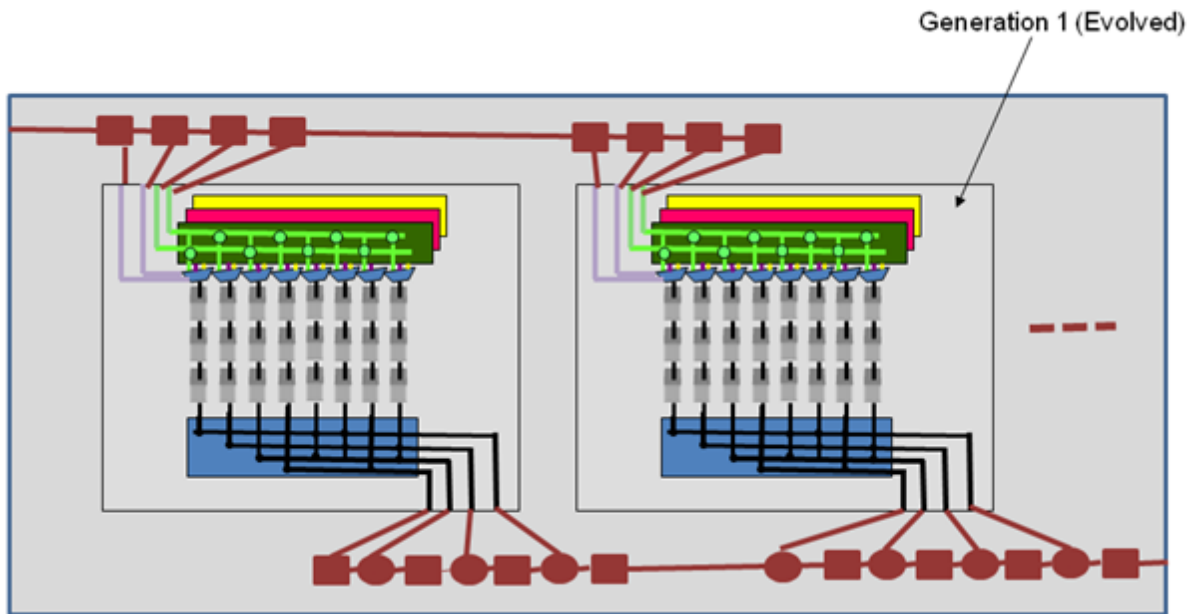


Figure 3 – Two cores with adaptive scan version G2 for pin-limited test consisting of a memory-less pipelined structure and combinational logic added on to adaptive scan.

Although Figure 3 shows the G2 being a layer on G1 technology there is opportunity to evolve the core compression block and serialization logic over time.

Evolution of adaptive scan ensures lower test cost while being easy-to-use.

Built-in Compression Synthesis Flow

While adaptive scan compression is shown to be effective and evolving, key to many design teams is the avoidance of productivity impact from design-for-test (DFT). Synopsys built-in standard scan synthesis methodology is widely used in conventional ASIC and SoC design flows in order to keep up with today’s design complexity, size, and testability considerations. Design and test must be addressed together throughout the entire design process rather than separately. That is, to successfully meet all the design goals of these immensely complex devices, including function, timing, area, power and testability, swift convergence of all requirements must be simultaneously attained.

DFTMAX compression enables RTL designers to take on the DFT tasks, including compression logic, by transparently implementing DFT during the design process, eliminating the need for highly specialized test knowledge. DFTMAX compression, a key element of Synopsys’ DFT closure strategy, makes DFT implementation transparent in the implementation flow, without interfering with the designers’ need to meet functional, timing and power requirements. Furthermore, DFT MAX compression works with DC Graphical to proactively minimize congestion. For maximum productivity with DFT MAX compression, test DRC and automatic test rule violation correction capabilities are tightly integrated within the built-in test environment.

DFT MAX compression enables RTL designers to quickly and accurately account for testability and resolve any test issues early in the design cycle, thus rapidly achieving their DFT goals without costly design iterations. Smooth, built-in DFT flows results in faster turn-around time compared to other flows that are unpredictable (see Figure 4).

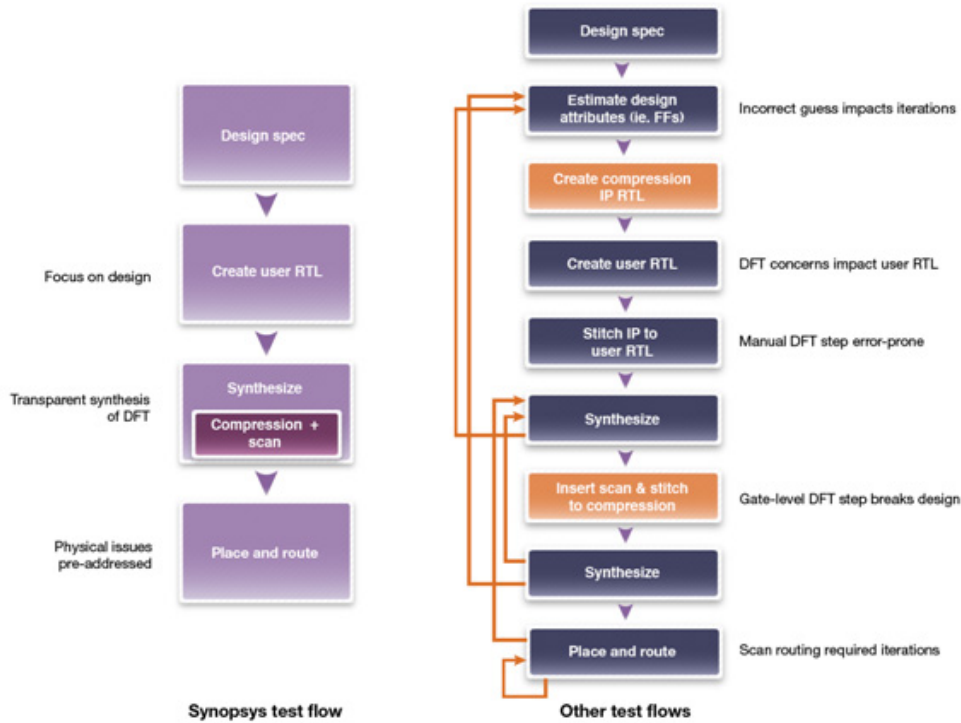


Figure 4 - Synopsys built-in test flow offer much faster turn-around time compared to other flows

Summary

DFTMAX compression contains powerful adaptive scan technology that reduces test costs of integrated circuits without negatively impacting the design flow. The reduction in test data volume and test application time can be used to increase the number of test patterns such that new defect mechanisms can be targeted for enhanced quality of test. With a unique architecture, adaptive scan retains all the benefits of standard scan solution, including for pin-limited test. Wide production use of DFTMAX compression provides both validation and direction for adaptive scan. Adaptive scan is technology that will keep adapting to the needs of the next generation designs.



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